SmartHCF™ Mobile Modem

Host-Controlled, V.90/K56flex™ Modem Device Set with Host Side Device (P9573), SmartDAA™ (20463), and Optional Voice Codec (20437) for PCI Bus/MiniPCI/CardBus-Based Mobile Applications

Designer's Guide (Preliminary)

Conexant Proprietary Information

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CONEXANT™

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1. INTRODUCTION

1.1 OVERVIEW

The Conexant™ SmartHCF Host-Controlled, V.90/K56flex Modem Device Family with SmartDAA technology supports analog data up to 56 kbps, analog fax to 14.4 kbps, telephone answering machine (TAM), voice/speakerphone (optional), and PCI Bus/MiniPCI/CardBus host interface operation. These modem devices meet the size and power requirements of the mobile environment. The modem operates with PSTN telephone lines in the U.S./Japan/Canada and optionally world-wide. Modem software is provided. Table 1-1 lists the available models.

Conexant's SmartDAA technology (patent pending) eliminates the need for a costly line transformer, relays, and opto-isolators typically used in discrete DAA (Data Access Arrangement) implementations. The SmartDAA architecture also simplifies product implementation by eliminating the need for country-specific board configurations enabling world-wide homologation of a single modem board design.

The SmartDAA system-powered DAA operates reliably without drawing power from the line, unlike line-powered DAAs which operate poorly when line current is insufficient due to long lines or poor line conditions. Enhanced features, such as monitoring of local extension status without going off-hook, are also supported.

Incorporating Conexant's proprietary Digital Isolation Barrier (DIB) design (patent pending) and other innovative DAA features, such as Digital PBX line protection and reporting, the SmartDAA architecture simplifies application design, minimizes layout area, and reduces component cost.

For over a decade, Conexant has assisted customers with DAA technology and homologation. This expertise and system level approach has been leveraged in this product.

The SmartHCF device set, consisting of a Host Side Device (HSD) in a 100-pin TQFP and a Line Side Device (LSD) (SmartDAA device) in a 32-pin TQFP, supports data/fax/TAM operation with hardware-based digital signal processing and DAA/telephone line interface functions (Figure 1-1). The optional Voice Codec (VC), in a 32-pin TQFP, supports voice/full-duplex speakerphone (FDSP) operation with interfaces to a microphone, speaker, and telephone handset/headset. Figure 1-2 identifies the major hardware signal interfaces.

In V.90/K56flex data mode, the modem can receive data at speeds up to 56 kbps from a digitally connected V.90 or K56flex-compatible central site modem. In this mode, the modem can transmit data at speeds up to V.34 rates.

In V.34 data mode, the modem operates at line speeds up to 33.6 kbps. When applicable, error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost average data throughput. Non-error-correcting mode is also supported.

Fax Group 3 send and receive rates are supported up to 14.4 kbps with T.30 protocol.

V.80 synchronous access mode supports host-controlled communication protocols, e. g., H.324 video conferencing.

Audio recording and playback over the telephone line interface using A-Law, μ-Law, or linear coding at 8 kHz sample rate supports applications such as remote digital telephone answering machine (TAM).

This designer's guide describes the modem hardware capabilities and identifies the supporting commands. Commands and parameters are defined in the Commands Reference Manual (Doc. No. 100498, formerly identified as Doc. No. 1118).

Table 1-1. SmartHCF Modem Models and Functions

Model/Order/Part Numbers					Supported Functions				
Marketing Name	Device Set Order No.	Host Side Device (HSD) [100-Pin TQFP] Part No.	Line Side Device (LSD) (SmartDAA) [32-Pin TQFP] Part No.	Voice Codec (VC) [32-Pin TQFP] Part No.	Host Bus	DAA Type	V.90/K56flex Data, V.17 Fax, TAM	World-Wide	Voice/ FDSP
SmartHCF/M-PCI	DS56-L153-081	P9573-11	20463-12	—	PCI	US/J/C	Y	—	—
SmartHCF/MS-PCI	DS56-L153-091	P9573-11	20463-12	20437-11	PCI	US/J/C	Y	—	Y
SmartHCF/MW-PCI	DS56-L153-101	P9573-11	20463-11	—	PCI	WW	Y	Y	—
SmartHCF/MWS-PCI	DS56-L153-111	P9573-11	20463-11	20437-11	PCI	WW	Y	Y	Y
SmartHCF/MC-CB	DS56-L153-121	P9573-21	20463-12	—	CardBus	US/J/C	Y	—	—
SmartHCF/MCS-CB	DS56-L153-131	P9573-21	20463-12	20437-11	CardBus	US/J/C	Y	—	Y
SmartHCF/MCW-CB	DS56-L153-141	P9573-21	20463-11	—	CardBus	WW	Y	Y	—
SmartHCF/MCWS-CB	DS56-L153-151	P9573-21	20463-11	20437-11	CardBus	WW	Y	Y	Y

Notes:

1. Model options:
   - M Mobile.
   - S Voice/full-duplex speakerphone (FDSP).
   - W World-wide.
   - -CB CardBus Interface.
   - -PCI PCI/MiniPCI Interface.
2. Supported functions (Y = Supported; – = Not supported):
   - TAM Telephone answering machine (Voice playback and record through telephone line)
   - FDSP Full-duplex speakerphone and voice playback and record through telephone line, handset, and mic/speaker
   - US/J/C U.S., Japan, Canada
   - WW World-wide.
3. Software configuration/functions determined by Device ID loaded into EEPROM (see Section 6.3.2).

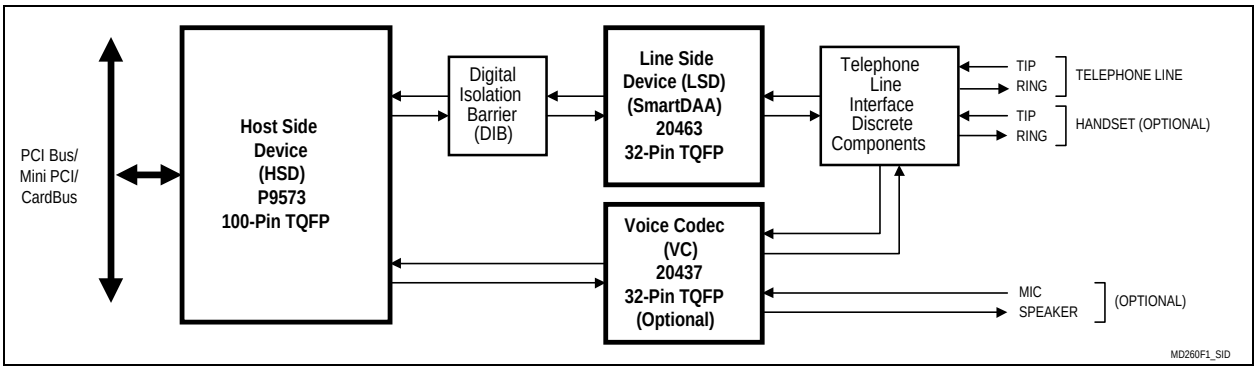

Figure 1-1. SmartHCF Modem Simplified Interface Diagram

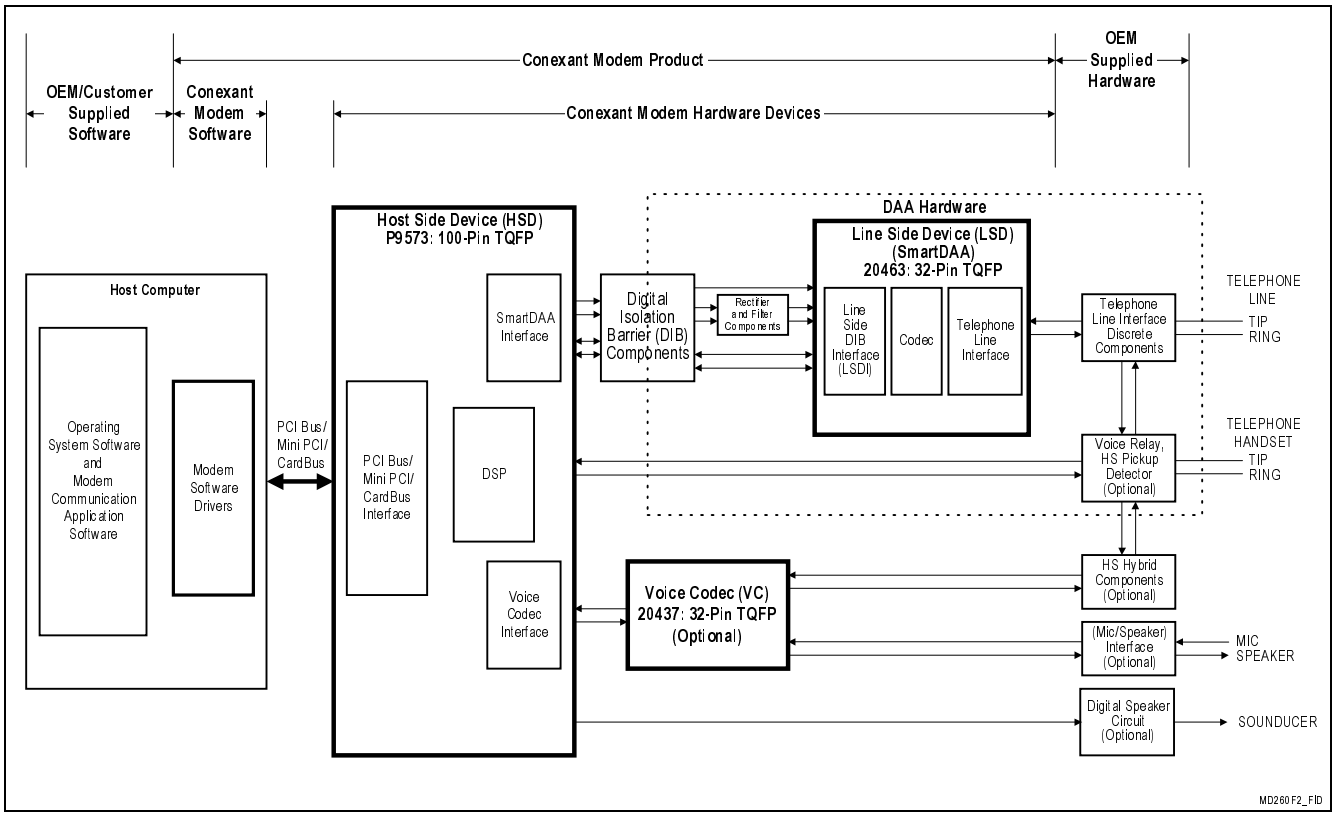

Figure 1-2. SmartHCF Modem Major Interfaces

1.2 FEATURES

1.2.1 General Modem Features

- V.90 data modem with receive rates up to 56k bps and send rates up to V.34 rates
  - ITU-T V.90, K56flex, V.34 (33.6 kbps), V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and 103
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - V.250 (ex V.25 ter) and V.251 (ex V.25 ter Annex A) commands
- V.17 fax modem with send and receive rates up to 14.4 kbps
  - V.17, V.29, V.27 ter, and V.21 ch 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0 commands
- Telephony/TAM
  - V.253 commands
  - 8-bit μ-Law/A-Law coding (G.711)
  - 8-bit/16-bit linear coding
  - 8 kHz sample rate
  - Concurrent DTMF, ring, and Caller ID detection
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- V.8/V.8bis and V.251 (ex V.25 ter Annex A) commands
- Data/Fax/Voice call discrimination
- Full-duplex Speakerphone (FDSP) Mode (S models)
  - Microphone and speaker interface
  - Telephone handset/headset interface
- Hardware-based digital signal processing
- Single configuration profile stored in host
- Operates in US/Japan/Canada
- World-wide operation (W models)
  - Complies to TBR21 and other country requirements
  - Caller ID detection
- System compatibilities
  - Windows 95, Windows 95 OSR2, Windows 98, Windows NT 4.0, Windows 2000 operating systems
  - Microsoft's PC 98 and PC 99 Design Initiative compliant
  - Advanced Configuration and Power Interface (ACPI)
  - Unimodem/V compliant
  - Pentium 133 MHz compatible PC or greater
  - 16 Mbyte RAM or more
- Thin packages support low profile designs
  - HSD (P9573): 100-pin TQFP (1.2 mm max. height)
  - LSD (20463): 32-pin TQFP (1.6 mm max. height)
  - VC (20437): 32-pin TQFP (1.6 mm max. height)
- +3.3V operation with +5V tolerant digital inputs

1.2.2 PCI Bus Host Interface Features

- 32-bit PCI Bus host interface
  - Meets PCI Local Bus Specification Rev. 2.2
  - PCI Bus Mastering interface
  - 33 MHz PCI clock support
- Supports Power Management
  - Meets PCI Bus Power Management Spec. Rev. 1.1
  - ACPI Power Management Registers
  - APM support
  - PME# support
  - Vaux/Vpci power switching support
  - VauxDET support

1.2.3 SmartDAA Features

- Digital PBX line protection
- System side powered DAA operates under poor line current supply conditions
- Wake-on-ring
- Ring detection
- Line polarity reversal detection
- Line current loss detection
- Caller ID (CID) detection
- Pulse dialing
- Line-in-use detection – detects even while on-hook
- Remote hang-up detect – for efficient call termination
- Extension pickup detect
- Call waiting detection
- Meets world-wide DC VI Masks requirements (W models)

1.2.4 Applications

- Laptop, notebook, and handheld computers
- PCI Bus/Mini-PCI embedded system boards
- PCI Bus/Mini-PCI/CardBus plug-in cards

1.3 TECHNICAL OVERVIEW

1.3.1 General Description

Modem operation, including dialing, call progress, telephone line interface, telephone handset interface, voice/speakerphone interface, and host interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

The modem hardware connects to the host processor via a PCI/MiniPCI/CardBus bus interface. The OEM adds a crystal circuit, EEPROM, DIB and LSD power rectifier and filter components, telephone line interface, optional telephone handset interface, optional voice/speakerphone interface, and other supporting discrete components as required by the modem model and the application to complete the system.

1.3.2 Host Modem Software

The host modem software performs the following tasks:

1. General modem control, which includes command sets, fax Class 1, TAM, voice/speakerphone, error correction, data compression, and operating system interface functions.
2. Modem data pump (MDP) control. Binary DSP executable code controlling MDP operation is downloaded as required during operation. Signal processing, including data and facsimile modulation and demodulation, as well as voice sample formatting, is performed in the hardware DSP.
3. SmartDAA control, which includes HSD SmartDAA Interface control, LSD configuration and control, telephone line interface parameter control, and telephone line impedance control.

Configurations of the modem software are provided to support modem models listed in Table 1-1.

1.3.3 Operating Modes

Data/Fax Modes

In V.90/K56flex data modem mode, the modem can receive data from a digital source using a V.90- or K56flex-compatible central site modem at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data at line speeds up to V.34 rates. This mode can fallback to full-duplex V.34 mode, and to lower rates, as dictated by line conditions.

In V.34 data modem mode, the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported.

In V.32 bis data modem mode, the modem can operate at line speeds up to 14.4 kbps.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the EIA/TIA-578 Class 1 or T.31 Class 1.0 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

Synchronous Access Mode (SAM) - Video Conferencing

V.80 Synchronous Access Mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

TAM Mode

TAM Mode features include 8-bit μ-Law, A-Law, and linear coding at 8 kHz sample rate. Full-duplex voice supports concurrent voice receive and transmit. Tone detection/generation, call discrimination, and concurrent DTMF detection are also supported. This mode supports applications such as digital TAM, voice annotation, and recording from and playback to the telephone line. ADPCM (4-bit IMA) coding is also supported to meet Microsoft WHQL logo requirements.

TAM Mode is supported by three submodes:

1. Online Voice Command Mode supports connection to the telephone line or, for S models, a microphone/speaker/handset/headset.
2. Voice Receive Mode supports recording voice or audio data input from the telephone line or, for S models, a microphone/handset/headset.
3. Voice Transmit Mode supports playback of voice or audio data to the telephone line or, for S models, a speaker/handset/headset.

Voice/Speakerphone Mode (S Models)

The S models include additional telephone handset, external microphone, and external speaker interfaces which support voice and full-duplex speakerphone (FDSP) operation.

Hands-free full-duplex telephone operation is supported in Speakerphone Mode under host control. Speakerphone Mode features an advanced proprietary speakerphone algorithm which supports full-duplex voice conversation with acoustic, line, and handset echo cancellation. Parameters are constantly adjusted to maintain stability with automatic fallback from full-duplex to pseudo-duplex operation. The speakerphone algorithm allows position independent placement of microphone and speaker. The host can separately control volume, muting, and AGC in microphone and speaker channels.

1.3.4 Reference Design

A MiniPCI Type IIIB data/fax/TAM reference design board is available to minimize application design time and costs.

The board is pretested to pass FCC Part 15, Part 68, and CTR 21 for immediate manufacturing.

A design package for the board is available in electronic form. The design package includes schematics, bill of materials (BOM), vendor parts list (VPL), board layout files in Gerber format, and complete documentation.

The design can also be used for the basis of a custom design by the OEM to accelerate design completion for rapid market entry.

1.4 HARDWARE DESCRIPTION

SmartDAA™ technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators that are typically used in discrete DAA implementations. The programmable SmartDAA architecture simplifies product implementation in world-wide markets by eliminating the need for country-specific components.

1.4.1 Host Side Device (HSD)

The HSD, packaged in a 100-pin TQFP, includes a PCI/MiniPCI/CardBus Interface, a Modem Data Pump (MDP), and a SmartDAA Interface.

The PCI/MiniPCI/CardBus interface connects directly to an embedded or external PCI/MiniPCI/CardBus interface eliminating the need for additional external logic components.

The MDP performs telephone line signal modulation/demodulation in a hardware digital signal processor (DSP) which reduces computational load on the host processor. Downloadable architecture allows updating of MDP executable code.

The SmartDAA Interface communicates with, and supplies power and clock to, the LSD through the DIB.

1.4.2 Digital Isolation Barrier (DIB) (OEM Supplied)

The DIB electrically DC isolates the HSD from the LSD and telephone line. The HSD is connected to a fixed digital ground and operates with standard CMOS logic levels. The LSD is connected to a floating ground and can tolerate high voltage input (compatible with telephone line and typical surge requirements).

The DIB power and clock transformer (PCXFMR) couples power and clock from the HSD to the LSD. (See Mobile Product Updates for qualified transformers.)

The DIB data channel supports bidirectional half-duplex serial transfer of data, control, and status information between the HSD and the LSD.

1.4.3 SmartDAA Line Side Device (LSD)

The LSD includes a Line Side DIB Interface (LSDI), a coder/decoder (codec), and a Telephone Line Interface (TLI).

The LSDI communicates with, and receives power and clock from, the SmartDAA interface in the HSD through the DIB.

LSD power is received from the DIB PCXFMR secondary winding through a half-wave rectifying diode and capacitive power filter circuit. The CLK input is also accepted from the PCXFMR secondary winding through a capacitor and a resistor in series.

Information is transferred between the LSD and the HSD through the DIB_P and DIB_N pins. These pins connect to the HSD DIB_DATAP and DIB_DATAN pins, respectively, through the DIB.

The TLI integrates DAA and direct telephone line interface functions and connects directly to the line TIP and RING pins, as well as to external line protection components.

Direct LSD connection to TIP and RING allows real-time measurement of telephone line parameters, such as the telephone central office (CO) battery voltage, individual telephone line (copper wire) resistance, and allows dynamic regulation of the off-hook TIP and RING voltage and total current drawn from the central office (CO). This allows the modem to maintain compliance with U.S. and world-wide regulations and to actively control the DAA power dissipation.

1.4.4 Voice Codec (VC) (S Models)

The optional VC, packaged in a 32-pin TQFP, supports voice/full-duplex speakerphone (FDSP) operation with interfaces to a microphone and speaker and to a telephone handset/headset.

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2. TECHNICAL SPECIFICATIONS

2.1 ESTABLISHING DATA MODEM CONNECTIONS

Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with ITU-T Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, and progress tones can be detected in accordance with the applicable standard represented by the country profile currently in affect.

Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible square wave input (frequency is country-dependent).

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for a period of time determined by country requirement to allow transmission of the billing signal.

Connection Speeds

Data modem line speed can be selected using the +MS command in accordance with V.25 ter. The +MS command selects modulation, enables/disables automode, and selects transmit and receive minimum and maximum line speeds.

Automode

Automode detection can be enabled by the +MS command to allow the modem to connect to a remote modem in accordance with V.25 ter.

2.2 DATA MODE

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

DTE-to-Modem Flow Control

If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

Escape Sequence Detection

The "+++" escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127.

GSTN Cleardown (V.90/K56flex, V.34, V.32 bis, V.32)

Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Fall Forward/Fallback (V.90/K56flex, V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within K56flex/V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS command.

When connected in V.90/K56flex/V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E1 command.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

2.3 ERROR CORRECTION AND DATA COMPRESSION

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

V.42 bis Data Compression

V.42 bis data compression mode operates when a LAPM or MNP connection is established.

The V.42 bis data compression employs a "string learning" algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two dictionaries, dynamically updated during normal operation, are used to store the strings.

MNP 5 Data Compression

MNP 5 data compression mode operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.4 FAX CLASS 1 OPERATION

Facsimile functions operate in response to Fax Class 1 commands when +FCLASS=1 or +FCLASS=1.0.

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.5 VOICE/TAM MODE

Voice and audio functions are supported by the Voice Mode. Voice Mode includes three submodes: Online Voice Command Mode, Voice Receive Mode, and Voice Transmit Mode.

2.5.1 Online Voice Command Mode

This mode results from the connection to the telephone line or a voice/audio I/O device (e.g., microphone or speaker) through the use of the +FCLASS=8 and +VLS commands. After mode entry, AT commands can be entered without aborting the connection.

2.5.2 Voice Receive Mode

This mode is entered when the +VRX command is active in order to record voice or audio data input, typically from a microphone or the telephone line.

Received analog voice samples are converted to digital form and compressed for reading by the host. AT commands control the codec sample rate.

Received analog mono audio samples are converted to digital form and formatted into 8-bit μ-Law, A Law, linear, or 4-bit IMA ADPCM format for reading by the host. AT commands control the bit length and sampling rate. Concurrent DTMF/tone detection is available.

2.5.3 Voice Transmit Mode

This mode is entered when the +VTX command is active in order to playback voice or audio data, typically to a speaker or to the telephone line. Concurrent DTMF/tone detection is available. Digitized audio data is converted to analog form.

2.5.4 Speakerphone Modes

Speakerphone modes are selected in voice mode with the following commands:

Speakerphone ON/OFF (+VSP). This command turns the Speakerphone function ON (+VSP = 1) or OFF (+VSP = 0).

Microphone Gain (+VGM=<gain>). This command sets the microphone gain of the Speakerphone function.

Speaker Gain (+VGS=<gain>). This command sets the speaker gain of the Speakerphone function.

2.6 FULL-DUPLEX SPEAKERPHONE (FDSP) MODE

The modem operates in FDSP mode when +FCLASS=8 and +VSP=1 (see 2.5.4).

In FDSP Mode, speech from a microphone or handset is converted to digital form, shaped, and output to the telephone line through the line interface circuit. Speech received from the telephone line is shaped, converted to analog form, and output to the speaker or handset. Shaping includes both acoustic and line echo cancellation.

2.7 CALLER ID

Caller ID can be enabled/disabled using the +VCID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem. The retrieval of the Caller ID via an explicit AT query at a later time is essential for implementing a compliant "Instantly available PC" concept.

2.8 MULTIPLE COUNTRY SUPPORT (W MODELS)

W models support modem operation in various countries. The country choice is made via the AT+GCI command or country select applet from within those installed in Windows registry. The following capabilities are provided in addition to the data modem functions previously described. Country dependent parameters are included in the .INF file for customization by the OEM Programmable Parameters

2.8.1 OEM Programmable Parameters

The following parameters are programmable:

- Dial tone detection levels and frequency ranges
- DTMF dialing transmit output level, DTMF signal duration, and DTMF interdigit interval parameters
- Pulse dialing parameters such as make/break times, set/clear times, and dial codes
- Ring detection frequency range
- Blind dialing disable/enable
- The maximum, minimum, and default carrier transmit level values
- Calling tone, generated in accordance with V.25, may also be disabled
- Call progress frequency and tone cadence for busy, ringback, congested, dial tone 1, and dial tone 2
- Answer tone detection period
- On-hook/off-hook, make/break, and set/clear relay control parameters

2.8.2 Blacklist Parameters

The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted"). Up to 20 such numbers may be tabulated. The blacklist parameters are programmable. The current blacklisted and delayed numbers can be queried via AT*B and AT*D commands, respectively.

2.9 DIAGNOSTICS

2.9.1 Commanded Tests

Diagnostics are performed in response to the &T1 command per V.54.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

Last Call Status Report (#UD). This command reports the status of the last call.

2.10 LOW POWER SLEEP MODE

When not connected in data, fax, or speakerphone mode, the HSD is placed in a low power state.

3. HARDWARE INTERFACE

3.1 HSD (P9573) HARDWARE PINS AND SIGNALS

3.1.1 HSD Signal Interfaces

PCI Bus/MiniPCI/CardBus Host Interface

The Host Side Device conforms to the PCI Local Bus Specification Version 2.2, MiniPCI Specification Draft 1.0, and PC Card Standard for CardBus. It is a memory slave and a bus master for PC host memory accesses (burst transactions). Configuration is by PCI configuration protocol.

The PCI Bus/MiniPCI/CardBus interface signals are:

- Address and data
  - 32 bidirectional Address/Data (AD[31-0]); bidirectional
  - 4 Bus Command and Byte Enable (CBE [3:0]); bidirectional
  - Bidirectional Parity (PAR); bidirectional
- Interface control
  - Cycle Frame (FRAME#); bidirectional
  - Initiator Ready (IRDY#); bidirectional
  - Target Ready (TRDY#); bidirectional
  - Stop (STOP#); bidirectional
  - Initialization Device Select (IDSEL); input
  - Device Select (DEVSEL#); bidirectional
- Arbitration
  - Request (REQ#); output
  - Grant (GRANT#); input
- Error reporting
  - Parity Error (PERR#); bidirectional
  - System Error (SERR#); bidirectional
- Interrupt
  - Interrupt A (INTA#); output
- System
  - Clock (PCICLK); input
  - Reset (PCIRST#); input
  - Clock Running (CLKRUN#); input
  - Power Management Event (PME#), output (-PCI model)
  - Status Change (STSCHG#), output (-CB model)

Power Detection and Switching

- Vaux Enable (VauxEN#); output (-PCI model)
- Vpci Enable (VpciEN#); output (-PCI model)
- Vpci Detect (VpciDET); input
- Vaux Detect (VauxDET); input

Serial EEPROM Interface

A serial EEPROM is required to store the Device ID, Vendor ID, Subsystem ID, Subsystem Vendor ID, and Power Management parameters for the PCI Configuration Space Header. The EEPROM is also required to store the CIS table for CardBus designs.

The EEPROM must be 2048 (128 x 16) bits or larger for PCI Bus/MiniPCI applications or 4096 (256 x 16) bits or larger for CardBus applications, and be rated at 1MHz (SROMCLK is 537.6 kHz). For example, the following EEPROMs or equivalent may be used: Microchip 93LC66B (256 x 16), 93LC56B (128 x 16), Atmel AT93C66 (256 x 16), AT93C56 (128 x 16). The EEPROM is programmable by the PC via the modem.

The EEPROM interface signals are:

- Serial Data Input (SROMIN); input
- Serial Data Output (SROMOUT); output
- Clock (SROMCLK); output
- Chip Select (SROMCS); output

LSD Interface (Through DIB)

The DIB interface signals are:

- Clock and Power Positive (PWRCLKP); output
- Clock and Power Negative (PWRCLKN); output
- Data Positive (DIB_DATAP); input/output
- Data Negative (DIB_DATAN); input/output

VC Interface (S Models)

The VC interface signals are:

- Modem Sleep (IASLEEP); output
- Master Clock (M_CLK); output
- Voice Serial Clock (V_SCLK); input
- Voice Serial Control (V_CTRL); output
- Voice Serial Frame Sync (V_STROBE); input
- Voice Serial Transmit Data (V_TXSIN); output
- Voice Serial Receive Data (V_RXOUT); input

Telephone Handset Interface (S Models)

The telephone handset interface signals are:

- Voice Relay Control (VOICE#); output
- Handset Pickup Detect (H_PICKUP); input

Call Progress Speaker Interface

The call progress speaker interface signal is:

- Digital speaker output (DSPKOUT); output

DSPKOUT is a square wave output in Data/Fax mode used for call progress or carrier monitoring. This output can be optionally connected to a low-cost on-board speaker, e.g., a sounducer, or to an analog speaker circuit.

3.1.2 HSD Interface Signals, Pin Assignments, and Signal Definitions

The HSD (P9573) 100-pin TQFP hardware interface signals are shown by major interface in Figure 3-1, are shown by pin number in Figure 3-2 and are listed by pin number in Table 3-1.

The HSD hardware interface signals are defined in Table 3-2.

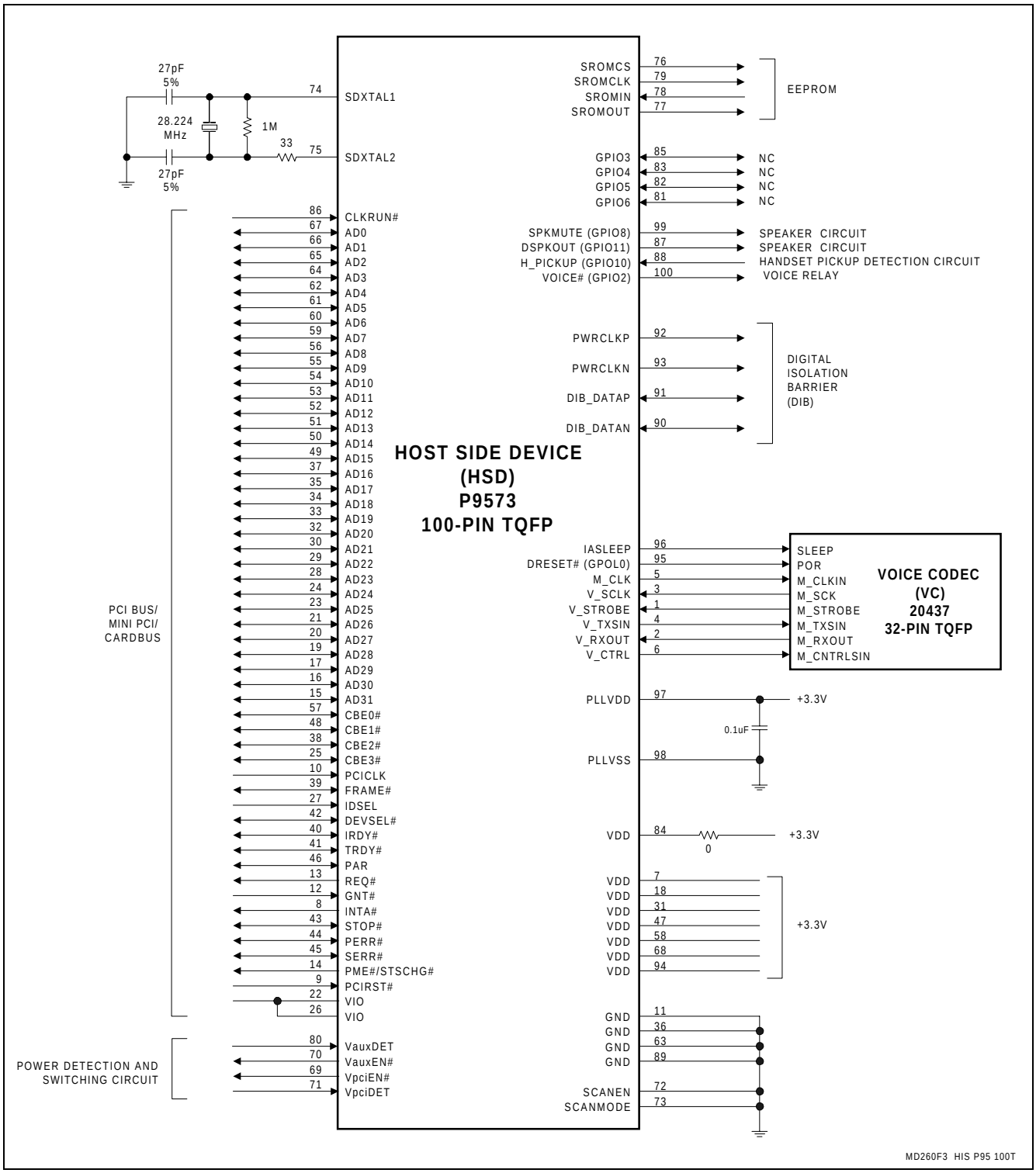

Figure 3-1. HSD (P9573) 100-Pin TQFP Hardware Interface Signals

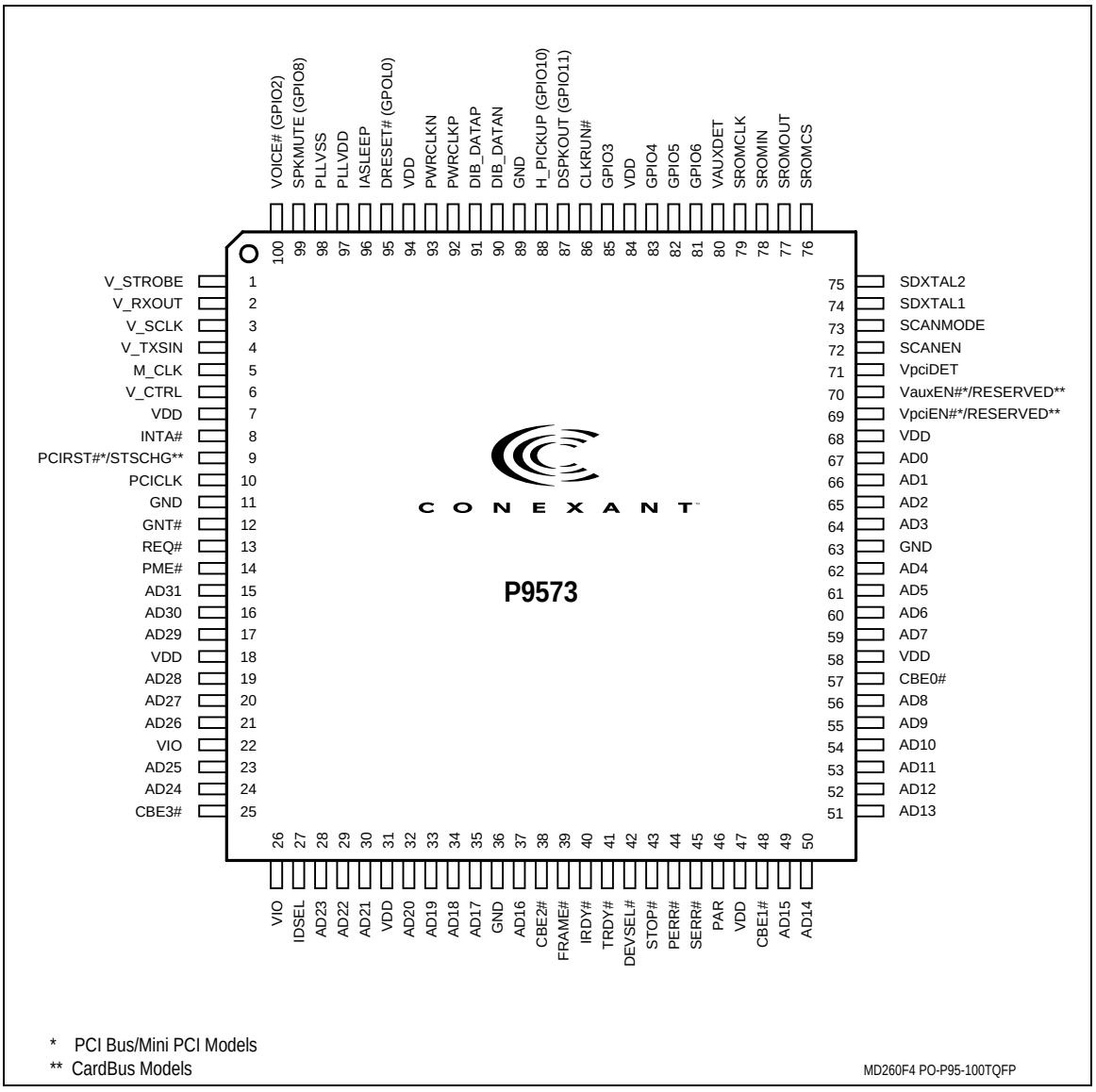

Figure 3-2. HSD (P9573) 100-Pin TQFP Pin Signals

Table 3-1. HSD (P9573) 100-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface	Pin	Signal Label	I/O Type	Interface
1	V_STROBE	Itpu	VC: M_STROBE	51	AD13	I/Opts	PCI Bus: AD13
2	V_RXOUT	Itk	VC: M_RXOUT	52	AD12	I/Opts	PCI Bus: AD12
3	V_SCLK	Itpu	VC: M_SCK	53	AD11	I/Opts	PCI Bus: AD11
4	V_TXSIN	Ot2	VC: M_TXSIN	54	AD10	I/Opts	PCI Bus: AD10
5	M_CLK	Ot2	VC: M_CLKIN	55	AD9	I/Opts	PCI Bus: AD9
6	V_CTRL	Ot2	VC: M_CNTRLSIN	56	AD8	I/Opts	PCI Bus: AD8
7	VDD	PWR	+3.3V	57	CBE0#	I/Opts	PCI Bus: CBE0#
8	INTA#	Opod	PCI Bus: INTA#	58	VDD	PWR	+3.3V
9	PCIRST#	Ip	PCI Bus: PCIRST#	59	AD7	I/Opts	PCI Bus: AD7
10	PCICLK	Ip	PCI Bus: PCICLK	60	AD6	I/Opts	PCI Bus: AD6
11	GND	GND	GND	61	AD5	I/Opts	PCI Bus: AD5
12	GNT#	Ipts	PCI Bus: GNT#	62	AD4	I/Opts	PCI Bus: AD4
13	REQ#	Opts	PCI Bus: REQ#	63	GND	GND	GND
14	PME#/STSCHG#	Opod	PCI Bus: PME# CardBus: STSCHG# (See Note 3)	64	AD3	I/Opts	PCI Bus: AD3
15	AD31	I/Opts	PCI Bus: AD31	65	AD2	I/Opts	PCI Bus: AD2
16	AD30	I/Opts	PCI Bus: AD30	66	AD1	I/Opts	PCI Bus: AD1
17	AD29	I/Opts	PCI Bus: AD29	67	AD0	I/Opts	PCI Bus: AD0
18	VDD	PWR	+3.3V	68	VDD	PWR	+3.3V
19	AD28	I/Opts	PCI Bus: AD28	69	VpciEN#/ RESERVED	Ot2	PCI Bus: Pwr Detection/Switching Ckt CardBus: Reserved (See Note 4)
20	AD27	I/Opts	PCI Bus: AD27	70	VauxEN#/ RESERVED	Ot2	PCI Bus: Pwr Detection/Switching Ckt CardBus: Reserved (See Note 4)
21	AD26	I/Opts	PCI Bus: AD26	71	VpciDET	Itpd	Pwr Detection/Switching Ckt
22	VIO	PWR	PCI Bus: VI/O	72	SCANEN	Itpd	GND
23	AD25	I/Opts	PCI Bus: AD25	73	SCANMODE	Itpd	GND
24	AD24	I/Opts	PCI Bus: AD24	74	SDXTAL1	Ix	Crystal or Clock Circuit
25	CBE3#	I/Opts	PCI Bus: CBE3#	75	SDXTAL2	Ox	Crystal or NC (if SDXTAL1 connected to Clock Circuit)
26	VIO	PWR	PCI Bus: VI/O	76	SROMCS	Ot2	SROM: Chip Select (CS)
27	IDSEL	Ip	PCI Bus: IDSEL	77	SROMOUT	Ot2	SROM: Data In (DI)
28	AD23	I/Opts	PCI Bus: AD23	78	SROMIN	Itpu	SROM: Data Out (DO)
29	AD22	I/Opts	PCI Bus: AD22	79	SROMCLK	Ot2	SROM: Clock (SK)
30	AD21	I/Opts	PCI Bus: AD21	80	VauxDET	Itpd	Pwr Detection/Switching Ckt
31	VDD	PWR	+3.3V	81	GPIO6	Itpu/Ot12	NC
32	AD20	I/Opts	PCI Bus: AD20	82	GPIO5	Itpu/Ot12	NC
33	AD19	I/Opts	PCI Bus: AD19	83	GPIO4	Itpu/Ot12	NC
34	AD18	I/Opts	PCI Bus: AD18	84	VDD	PWR	+3.3V through 0 Ω resistor
35	AD17	I/Opts	PCI Bus: AD17	85	GPIO3	Itpu/Ot12	NC
36	GND	GND	GND	86	CLKRUN#	I/Opod	PCI Bus: CLKRUN#
37	AD16	I/Opts	PCI Bus: AD16	87	DSPKOUT (GPIO11)	Ot12	AI: Digital/analog speaker circuit for call progress
38	CBE2#	I/Opts	PCI Bus: CBE2#	88	H_PICKUP (GPIO10)	Itpu	Line Interface: Handset Pickup Detection Circuit
39	FRAME#	I/Opsts	PCI Bus: FRAME#	89	GND	GND	GND
40	IRDY#	I/Opsts	PCI Bus: IRDY#	90	DIB_DATAN	Idd/Odd	DIB: Data Negative Channel
41	TRDY#	I/Opsts	PCI Bus: TRDY#	91	DIB_DATAP	Idd/Odd	DIB: Data Positive Channel
42	DEVSEL#	I/Opsts	PCI Bus: DEVSEL#	92	PWRCLKP	Odpc	DIB: PCXFMR primary winding top
43	STOP#	I/Opsts	PCI Bus: STOP#	93	PWRCLKN	Odpc	DIB: PCXFMR primary winding bottom
44	PERR#	I/Opsts	PCI Bus: PERR#	94	VDD	PWR	+3.3V
45	SERR#	I/Opod	PCI Bus: SERR#	95	DRESET# (GPOL0)	Ot2	VC: POR
46	PAR	I/Opts	PCI Bus: PAR	96	IASLEEP	Ot2	VC: SLEEP
47	VDD	PWR	+3.3V	97	PLLVDD	PWR	+3.3V and to GND through 0.1 µF
48	CBE1#	I/Opts	PCI Bus: CBE1#	98	PLLVSS	GND	GND
49	AD15	I/Opts	PCI Bus: AD15	99	SPKMUTE (GPIO8)	It/Ot12	Audio Circuit: Spkr Control (output); Vaux Mode Power Select (input)
50	AD14	I/Opts	PCI Bus: AD14	100	VOICE# (GPIO2)	Ot12	Line Interface: Voice Relay Control

Table 3-1. HSD (P9573) 100-Pin TQFP Pin Signals (Cont'd)

Notes:

1. I/O Types

I/Opod	Digital input/output, PCI, open drain (PCI type = o/d)
I/Opsts	Digital input/output, PCI, sustained tristate (PCI type = s/t/s)
I/Opts	Digital input/output, PCI, tristate (PCI type = t/s)
Idd	input, DIB, data channel
Ip	Digital input, PCI, totem pole (PCI type = in)
Ipts	Digital input, PCI, (PCI type = t/s)
It	Digital input, TTL-compatible
Itk	Digital input, TTL-compatible, internal keeper
Itpd	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-up
It/Ot2	Digital input, TTL-compatible/digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
It/Ot12	Digital input, TTL-compatible/digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ix	Crystal/clock input
Odpc	Output, DIB power and clock channel
Odd	Output, DIB data channel
Ood	Digital output, open drain
Opod	Digital output, PCI, open drain (PCI type =o/d)
Opts	Digital output, PCI, tristate (PCI type = t/s)
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ox	Crystal output

2. Interface Legend:

NC	No internal pin connection
DIB	Digital Isolation Barrier
VC	Voice Codec

3. PME#/STSCHG# pin:
   - PME# supported by P9573-11;
   - STSCHG# supported by P9573-21.

4. VauxEN#/RESERVED and VpciEN#/RESERVED pins:
   - VauxEN# and VpciEN# supported by P9573-11;
   - RESERVED supported by P9573-21.

5. All references to PCI Bus also apply to MiniPCI and CardBus unless otherwise specified.

Table 3-2. HSD (P9573) 100-pin TQFP Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
SYSTEM			
SDXTAL1 SDXTAL2	74 75	Ix Ox	**Crystal/Clock In and Crystal Out.** Connect SDXTAL1 to a 28.224000 MHz crystal or clock circuit. Connect SDXTAL2 to the 28.224000 MHz crystal circuit or leave open if SDXTAL1 is connected to a clock circuit. (See layout guidelines in Section 5.)
VDD	7, 18, 31, 47, 58, 68, 94	PWR	**Digital Supply Voltage.** Connect to +3.3V.
VDD	84	PWR	**Digital Supply Voltage.** Connect to +3.3V through a 0 Ω resistor. **Note**: Pin 84 connection to +3.3V through a resistor allows a common board design to be used with either the SmartHCF P9573 device (pin 84 [VDD] connects to +3.3V through 0 Ω) or the SmartHSF 11242 device (pin 84 [LP_CLK] connects to +3.3V through 240 KΩ).
GND	11, 36, 63, 89	GND	**Digital Ground.** Connect to digital ground.
VIO	22, 26	PWR	**I/O Signaling Voltage Reference.** Connect to PCI Bus VI/O. Used internally for PCI clamping.
PLLVDD	97	PWR	**Digital Supply Voltage.** Connect to +3.3V and to GND through 0.1 µF.
PLLGND	98	GND	**Digital Ground.** Connect to digital ground.
SCANEN	72	Itpd	**Scan Enable.** Connect to GND.
SCANMODE	73	Itpd	**Scan Mode**. Connect to GND.
CLKRUN#	86	I/Opod, (o/d)	**Clock Running.** CLKRUN# is an input used to determine the status of CLK and an open drain output used to request starting or speeding up CLK. Connect to GND for PCI Bus designs. Connect to MiniPCI/CardBus CLKRUN# pin for MiniPCI/CardBus designs.
POWER DETECTION AND SWITCHING			
VauxEN#	70	Ot2	**Vaux Enable.** Active low output used to enable Vaux FET. For use in designs that switch between Vaux and Vpci for different power states and for retail designs where the target PC may or may not support Vaux. (P9573-11 only.)
VpciEN#	69	Ot2	**Vpci Enable.** Active low output used to enable Vpci FET. For use in designs that switch between Vaux and Vpci for different power states and for retail designs where the target PC may or may not support Vaux. (P9573-11 only.)
VpciDET	71	Itpd	**Vpci Detect.** The VpciDET input indicates when PCI cycles and PCIRST# are to be ignored. Connect this pin to the PCI Bus +5V pins for PCI Bus designs, PCI 3.3V for MiniPCI designs, or to CardBus +3.3V pins for CardBus designs. VpciDET is deasserted when the PCI Bus enters the B3 state. This pin may alternatively be directly driven in embedded designs by using a logical signal, either +5V or +3.3V level, to indicate when the PCI Bus is in a B3 state. Driving this pin low synchronously to the PCI clock or when the PCI clock is stopped also allows the HSD to be put into a very low power mode. Therefore, using this method, if modem operation is not required, modem power consumption can be reduced even while the PCI Bus is in power state B0.
VauxDET	80	Itpd	**Vaux Detect.** Active high input used to detect the presence of Vaux. Connect to PCI Bus: Vaux. At device power on (POR), if D3_Cold bit in the EEPROM is a 1, PMC[15] is set to a 1 if VauxDET is high or PMC[15] is cleared to a 0 if VauxDET is low.
SERIAL EEPROM INTERFACE			
SROMCLK	79	Ot2	**Serial ROM Shift Clock.** Connect to SROM SK input (frequency: 537.6 kHz).
SROMCS	76	Ot2	**Serial ROM Chip Select.** Connect to SROM CS input.
SROMIN	78	Itpu	**Serial ROM Device Status and Data Out.** Connect to SROM DO output, through 1k Ω if using a +5V EEPROM.
SROMOUT	77	Ot2	**Serial ROM Instruction, Address, and Data In.** Connect to SROM DI input.

Table 3-2. HSD (P9573) 100-pin TQFP Signal Definitions (Cont'd)

Label	Pin	I/O Type	Signal Name/Description
PCI BUS INTERFACE			
PCICLK	10	Ip (in)	**PCI Bus Clock.** The PCICLK (PCI Bus CLK signal) input provides timing for all transactions on PCI. Connect to PCI Bus: CLK.
PCIRST#	9	Ip (in)	**PCI Bus Reset.** Active low input asserted to initialize PCI-specific registers, sequencers, and signals to a consistent reset state. Connect to PCI Bus: RST#.
AD[31:0]	15-17, 19-21, 23-24, 28-30, 32-35, 37, 49-56, 59-62, 64-67	I/Opts (t/s)	**Multiplexed Address and Data.** Address and Data are multiplexed on the same PCI pins. Connect to PCI Bus: AD[31-0].
CBE0# CBE1# CBE2# CBE3#	57 48 38 25	I/Opts (t/s)	**Bus Command and Bus Enable.** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, CBE[3:0]# define the bus command. During the data phase, CBE[3:0]# are used as Byte Enables. Connect to PCI Bus: CBE[3:0]#.
PAR	46	I/Opts (t/s)	**Parity.** Parity is even parity across AD[31:00] and CBE[3:0]#. The master drives PAR for address and write data phases; the Bus Interface drives PAR for read data phases. Connect to PCI Bus: PAR.
FRAME#	39	I/Opsts (s/t/s)	**Cycle Frame.** FRAME# is driven by the current master to indicate the beginning and duration of an access. Connect to PCI Bus: FRAME#.
IRDY#	40	I/Opsts (s/t/s)	**Initiator Ready.** IRDY# is used to indicate the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. Connect to PCI Bus: IRDY#.
TRDY#	41	I/Opsts (s/t/s)	**Target Ready.** TRDY# is used to indicate s the Bus Interface's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. Connect to PCI Bus: TRDY#.
STOP#	43	I/Opsts (s/t/s)	**Stop.** STOP# is asserted to indicate the Bus Interface is requesting the master to stop the current transaction. Connect to PCI Bus: STOP#.
IDSEL	27	Ip (in)	**Initialization Device.** IDSEL input is used as a chip select during configuration read and write transactions. Connect to PCI Bus: IDSEL.
DEVSEL#	42	I/Opsts (s/t/s)	**Device Select.** When actively driven, DEVSEL# indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected. Connect to PCI Bus: DEVSEL#.
REQ#	13	Opts (t/s)	**Reques**t. REQ# is used to indicate to the arbiter that this agent desires use of the bus. Connect to PCI Bus: REQ#.
GNT#	12	Ipts (t/s)	**Grant.** GNT# is used to indicate to the agent that access to the bus has been granted. Connect to PCI Bus: GNT#.
PERR#	44	I/Opsts (s/t/s)	**Parity Error.** PERR# is used for the reporting of data parity errors. Connect to PCI Bus: PERR#.
SERR#	45	Opod (o/d)	**System Error.** SERR# is an open drain output asserted to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. Connect to PCI Bus: SERR#.
INTA#	8	Opod (o/d)	**Interrupt A.** INTA# is an open drain output asserted to request an interrupt. Connect to PCI Bus: INTA#.
PME#	14	Opod (o/d)	**Power Management Event.** Active low open drain or active high TTL output (selected by the PME DRV bit in the EEPROM) asserted when a valid ring signal is detected and the PME_En bit of the PMCSR is a 1. This signal should be used only if the target PCI Bus supports power management wake-up event. Connect to the PCI Bus: PME#. (P9573-11 only.)
STSCHG#	14	Opod (o/d)	**Status Changed.** Active low output asserted to alert the host to changes in the RRdy/-Bsy bit (PRR1) in the Pin Replacement Register (PRR) and to the setting of the ReqAttn bit (ESR4) in the Extended Status Register (ESR). (P9573-12 only.)

Table 3-2. HSD (P9573) 100-pin TQFP Signal Definitions (Cont'd)

Label	Pin	I/O Type	Signal Name/Description
AUDIO INTERFACE			
DSPKOUT (GPIO11)	87	Ot12	**Call Progress (Digital Speaker) Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator. This signal is used for call progress or carrier monitoring. This output can be optionally connected to a low-cost on-board speaker, e.g., a sounducer, or to an analog speaker circuit.
SPKMUTE (GPIO8)	99	It/Ot12	**Speaker Mute/Vaux Mode Power Select.** Output (typically active low) used to turn off (mute) the speaker during normal operation. Applicable to S models only. Upon device reset, this pin is temporarily an input and is sampled. If sampled high and VauxDET is high, VpciEN# will be asserted when the device is in D0. If sampled low (e.g., SPKMUTE signal is pulled down to GND through 10k Ω) and VauxDET is high, VauxEN# will be asserted when the device is in D0. VauxEN# is always asserted when VauxDET is high in D3 with PME enabled. Either VauxEN# or VpciEN#, but not both, can be asserted at the same time.
TELEPHONE LINE (DAA)/AUDIO INTERFACE			
VOICE# (GPIO2)	100	Ot12	**Voice Relay Control.** Output (typically active low) used to control the normally open voice relay. The polarity of this output is configurable.
H_PICKUP (GPIO10)	88	Itpu	**Handset Pickup Detect.** Active high input indicating handset pickup.
DIB INTERFACE			
PWRCLKP	92	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD**.** Connect to DIB PCXFMR primary winding top.
PWRCLKN	93	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD**.** Connect to DIB PCXFMR primary winding bottom.
DIB_DATAP	91	Idd/Odd	**Data Positive.** Transfers data, control, and status information between HSD and LSD**.** Connect to LSD through DIB data positive channel components.
DIB_DATAN	90	Idd/Odd	**Data Negative.** Transfers data, control, and status information between HSD and LSD. Connect to LSD through DIB data negative channel components.
GPIO INTERFACE			
GPIO6	81	Itpu/Ot12	**Reserved.**
GPIO5	82	Itpu/Ot12	**Reserved.**
GPIO4	83	Itpu/Ot12	**Reserved.**
GPIO3	85	Itpu/Ot12	**Reserved.**

Table 3-2. HSD (P9573) 100-Pin TQFP Signal Definitions (Cont'd)

Label	Pin	I/O Type	Signal Name/Description
VOICE CODEC (VC) INTERCONNECT			
IASLEEP	96	Ot2	**Modem Sleep.** Connect to VC SLEEP pin.
DRESET# (GPOL0)	95	Ot2	**Modem Reset.** Connect to VC POR pin.
M_CLK	5	Ot2	**Master Clock Output**. Connect to VC M_CLKIN pin.
V_SCLK	3	Itpu	**Voice Serial Clock input.** Connect to VC M_SCK pin.
V_STROBE	1	Itpu	**Voice Serial Frame Sync Input.** Connect to VC M_STROBE pin.
V_CTRL	6	Ot2	**Voice Control Output.** Connect to VC M_CNTRLSIN pin.
V_TXSIN	4	Ot2	**Voice Serial Transmit Data Output.** Connect to VC M_TXSIN pin.
V_RXOUT	2	It	**Voice Serial Receive Data Input.** Connect to VC M_RXOUT pin.

Notes:

1. I/O Types

I/Opod	Digital input/output, PCI, open drain (PCI type = o/d)
I/Opsts	Digital input/output, PCI, sustained tristate (PCI type = s/t/s)
I/Opts	Digital input/output, PCI, tristate (PCI type = t/s)
Idd	input, DIB, data channel
Ip	Digital input, PCI, totem pole (PCI type = in)
Ipts	Digital input, PCI, (PCI type = t/s)
It	Digital input, TTL-compatible
Itpd	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-up
It/Ot2	Digital input, TTL-compatible/digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
It/Ot12	Digital input, TTL-compatible/digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ix	Crystal/clock input
Odpc	Output, DIB power and clock channel
Odd	Output, DIB data channel
Ood	Digital output, open drain
Opod	Digital output, PCI, open drain (PCI type =o/d)
Opts	Digital output, PCI, tristate (PCI type = t/s)
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Ox	Crystal output

2. Interface Legend:

NC = No internal pin connection

RESERVED = No external connection allowed (may have internal connection).

5. All references to PCI Bus also apply to MiniPCI and CardBus unless otherwise specified.

3.2 LSD (20463) HARDWARE PINS AND SIGNALS

3.2.1 LSD Signal Interfaces

HSD Interface (Through DIB)

The DIB interface signals are:

- Clock (CLK); input
- Digital Power (PWR+); input power
- Digital Ground (DGND); digital ground
- Data Positive (DIB_P); input
- Data Negative (DIB_N); input

Telephone Line Interface

The telephone line interface signals are:

- RING AC Coupled (RAC1); input
- TIP AC Coupled (TAC1); input
- Electronic Inductor Resistor (EIR); output
- TIP and RING DC Measurement (TRDC); input
- DAC Output Voltage (DAC); output
- Electronic Inductor Capacitor (EIC)
- Electronic Inductor Output (EIO)
- Electronic Inductor Feedback (EIF)
- Resistive Divider Midpoint (DCF)
- Transmit Analog Output (TXA); output
- Receive Analog Input (RXI); input
- Receiver Gain (RXG); output
- MOV Enable (MOVEN); output
- World-wide Impedance 0 (ZW0); input
- US Impedance 0 (ZUS0); input
- Transmit Feedback (TXF); input
- Transmit Output (TXO); output

3.2.2 LSD Interface Signals, Pin Assignments, and Signal Definitions

The LSD (20463) 32-pin TQFP hardware interface signals are shown by major interface in Figure 3-3, are shown by pin number in Figure 3-4, and are listed by pin number in Table 3-3.

The LSD hardware interface signals are defined in Table 3-4.

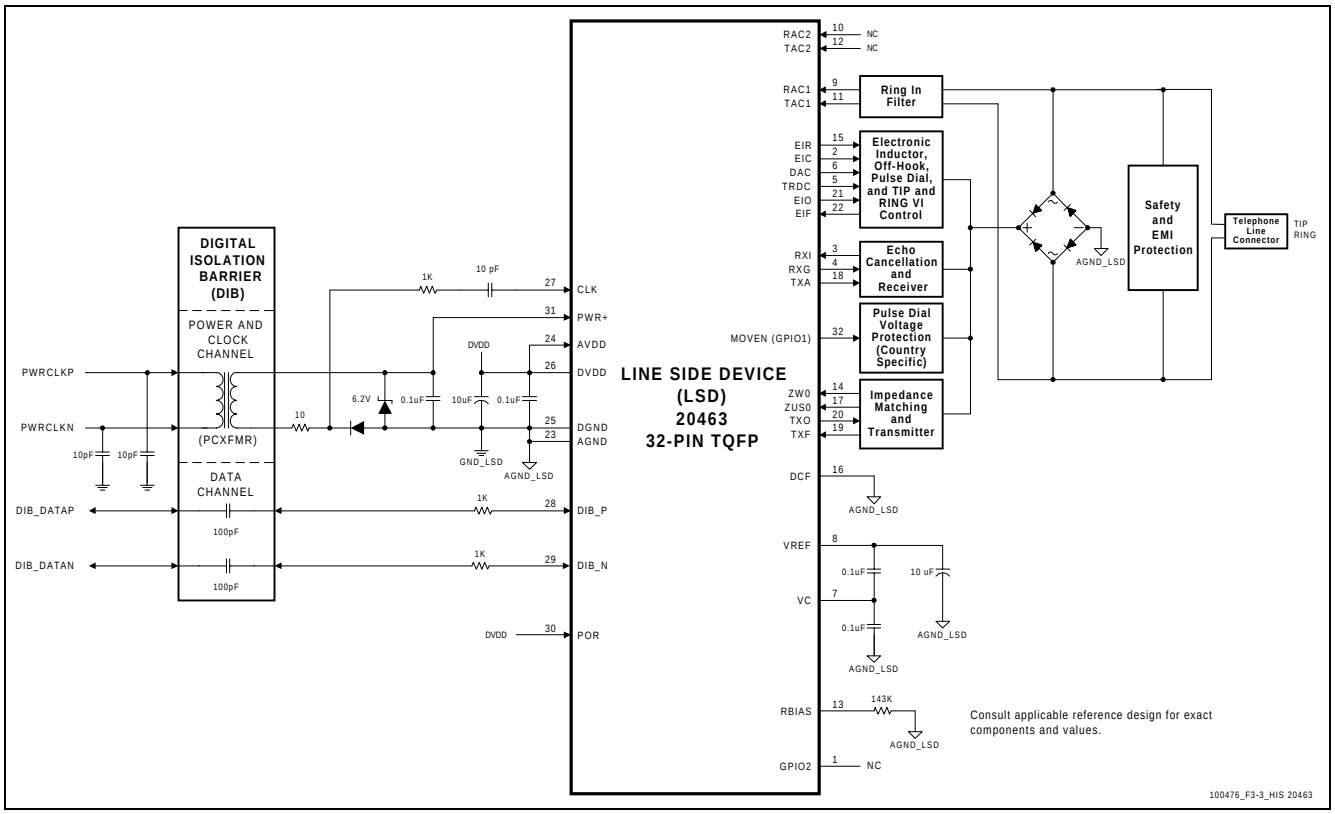

Figure 3-3. LSD (20463) 32-Pin TQFP Hardware Interface Signals

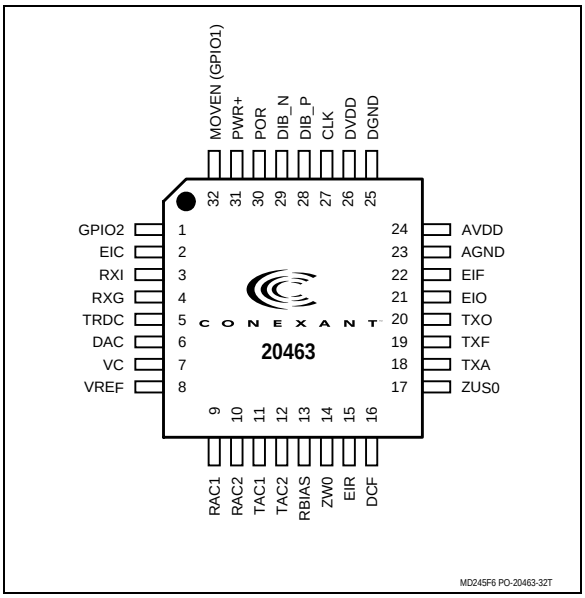

Figure 3-4. LSD (20463) 32-Pin TQFP Pin Signals

Table 3-3. LSD (20463) 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O Type	Interface
1	GPIO2	It/Ot12	NC
2	EIC	Oa	Telephone Line Interface Components
3	RXI	Ia	Telephone Line Interface Components
4	RXG	Oa	Telephone Line Interface Components
5	TRDC	Oa	Telephone Line Interface Components
6	DAC	Oa	Telephone Line Interface Components
7	VC	REF	VREF through 0.1 µF and to AGND_LSD through 0.1 µF
8	VREF	REF	VC through 0.1 µF and to AGND_LSD through 10 µF
9	RAC1	Ia	RING through 1 MΩ and 0.033 µF
10	RAC2	Ia	NC
11	TAC1	Ia	TIP through 1 MΩ and 0.033 µF
12	TAC2	Ia	NC
13	RBIAS	Ia	AGND_LSD through 143 KΩ
14	ZW0	Ia	Telephone Line Interface Components
15	EIR	Ot12	Telephone Line Interface Components
16	DCF	Ia	AGND_LSD
17	ZUS0	Ia	Telephone Line Interface Components
18	TXA	Oa	Telephone Line Interface Components
19	TXF	Ia	Telephone Line Interface Components
20	TXO	Oa	Telephone Line Interface Components
21	EIO	Oa	Telephone Line Interface Components
22	EIF	Ia	Telephone Line Interface Components
23	AGND	AGND_LSD	AGND_LSD
24	AVDD	PWR	LSD DVDD pin
25	DGND	GND_LSD	DIB PCXFMR secondary winding bottom through diode and 10 Ω in series and to GND_LSD
26	DVDD	PWR	LSD AVDD pin and to GND_LSD through 10 µF and 0.1 µF in parallel
27	CLK	I	DIB PCXFMR secondary winding bottom through 10 pF and 1 KΩ in series and through 10 Ω shared with LSD DGND pin through diode
28	DIB_P	I/O	DIB line side Data Positive capacitor through 1 KΩ
29	DIB_N	I/O	DIB line side Data Negative capacitor through 1 KΩ
30	POR	It	LSD DVDD pin
31	PWR+	PWR	DIB PCXFMR secondary winding top and to GND_LSD through 6.2 V zener diode and 0.1 µF in parallel
32	MOVEN (GPIO1)	Ot12	Telephone Line Interface Components

Notes:

1. I/O types*:
   - Ia — Analog input
   - It — Digital input, TTL-compatible
   - Oa — Analog output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - AGND_LSD — Isolated LSD Analog Ground
   - GND_LSD — Isolated LSD Digital Ground
2. Interface Legend:
   - HSD — Host Side Device

Table 3-4. LSD (20463) 32-Pin TQFP Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
SYSTEM SIGNALS			
AVDD	24	PWR	**Analog Power Supply.** Connect to the LSD DVDD pin. See layout guidelines in Section 5.
AGND	23	AGND_LSD	**LSD Analog Ground. LSD Analog Ground.** Connect to AGND_LSD at the GND_LSD/AGND_LSD tie point and to the analog ground plane. See layout guidelines in Section 5.
POR	30	It	**Power-On Reset.** Connect to LSD DVDD pin.
VREF	8	REF	**Output Reference Voltage.** Connect to VC through 0.1 µF and to AGND_LSD through 10 µF. Ensure a very close proximity between this capacitor and the VREF pin.
VC	7	REF	**Output Middle Reference Voltage.** Connect to AGND_LSD through 0.1 µF. Ensure a very close proximity between this capacitor and the VC pin. Use a short path and a wide trace to AGND_LSD pin.
DIB INTERFACE SIGNALS			
CLK	27	I	**Clock.** Provides input clock, AC coupled, to the LSD**.** Connect to DIB PCXFMR secondary winding bottom through 1 KΩ and 10 pF in series and through 10 Ω shared with LSD DGND pin through diode.
PWR+	31	PWR	**Digital Power Input**. Provides input digital power to the LSD. Connect to DIB PCXFMR secondary winding top, and to GND_LSD though a 6.2 V zener diode and 0.1 µF in parallel.
DVDD	26	PWR	**Digital Power**. Connect to pin 24 (AVDD) and to GND_LSD through 10 µF and 0.1 µF in parallel.
DGND	25	GND_LSD	**LSD Digital Ground.** Connect to DIB PCXFMR secondary winding bottom through diode in series with 10 Ω, and to GND_LSD at the GND_LSD/AGND_LSD tie point.
DIB_P, DIB_N	28, 29	I/O, I/O	**Data and Control Positive and Negative.** Connect to HSD DIB_DATAP and HSD DIB_DATAN, respectively, each line serially through 1 KΩ on LSD side and 100 pF in DIB. Signals are differential, and ping pong between DIB and HSD (half duplex).
TIP AND RING INTERFACE			
RAC1, TAC1	9, 11	Ia, Ia	**RING1 AC Coupled and TIP1 AC Coupled.** AC coupled voltage from telephone line used to detect ring. Connect RAC1 to the top of the diode bridge through 1 MΩ and 0.033 µF (200V). Connect TAC1 to the of the diode bridge through 1 MΩ and 0.033 µF (200V).
RAC2 TAC2	10, 12	Ia, Ia	**RING2 AC Coupled and TIP2 AC Coupled.** Not used. Leave open.
EIR	15	Oa	**Electronic Inductor Resistor.** Electronic inductor resistor switch.
EIC	2	Oa	**Electronic Inductor Capacitor Switch.** Internally switched to no connect when pulse dialing and to ground all other times. This is needed to eliminate pulse dial interference from the electronic inductor AC filter capacitor.
DAC	6	Oa	**DAC Output Voltage.** Output voltage of the reference DAC.
TRDC	5	Ia	**TIP and RING DC Measurement.** Input on-hook voltage (from a resistive divider). Used internally to extract TIP and RING DC voltage and Line Polarity Reversal (LPR) information.
EIO	21	Oa	**Electronic Inductor Output.** Calculated voltage is applied to this output to control offhook, pulse dial, and DC IV mask operation.
EIF	22	Ia	**Electronic Inductor Feedback.** Electronic inductor feedback.
RXG	4	Oa	**Receiver Gain.** Receiver gain output.
RXI	3	Ia	**Receive Analog Input.** Receive signal input.
TXA	18	Oa	**Transmit Analog Output.** Transmit signal used for canceling echo in the receive path.
MOVEN (GPIO1)	32	Ot12	**MOV Enable**. Connect to pulse dial voltage protection circuit for Australia/Poland/Italy use. Leave open if not required.
RBIAS	13	Ia	**Receiver Bias.** Connect to GND through 143 KΩ.
DCF	16	Ia	**Resistive Divider Midpoint.** Connect to LSD analog ground.

Table 3-4. LSD (20463) 32-Pin TQFP Pin Signal Definitions (Cont'd)

Label	Pin	I/O Type	Signal Name/Description
TIP AND RING INTERFACE (CONTINUED)			
ZW0	14	Ia	**World-Wide Impedance 0.** Input signal used to provide line complex impedance matching for world-wide countries.
ZUS0	17	Ia	**US Impedance 0.** Input signal used to provide line impedance matching for U.S.
TXO	20	Oa	**Transmit Output.** Outputs transmit signal and impedance matching signal; connect to transmitter transistor.
TXF	19	Ia	**Transmit Feedback.** Connect to emitter of transmitter transistor.
NOT USED			
GPIO2	1	It/Ot12	**General Purpose I/O 2**. Leave open if not used.

Notes:

1. I/O types*:
   - Ia — Analog input
   - It — Digital input, TTL-compatible
   - Oa — Analog output
   - Ot12 — Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
   - AGND_LSD — Isolated LSD Analog Ground
   - GND_LSD — Isolated LSD Digital Ground
   - *See LSD (20463) Digital Electrical Characteristics (Table 3-5)
2. Interface Legend:
   - HSD — Host Side Device
3. Interface components may vary (see reference design for exact components and values).

Table 3-5. LSD (20463) Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IN}	-0.30	–	3.60	V	VDD = +3.6V
Input Voltage Low	V_{IL}	–	–	1.0	V	
Input Voltage High	V_{IH}	1.6	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.33	V	
Output Voltage High	V_{OH}	2.97	–	–	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
GPIO Output Sink Current at 0.4 V maximum	–	2.4	–	-	mA	
GPIO Output Source Current at 2.97 V minimum	–	2.4	–	-	mA	
GPIO Rise Time/Fall Time		20		100	ns	

Test conditions unless otherwise noted:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF

3.3 VC (20437) HARDWARE PINS AND SIGNALS (S MODELS)

Microphone and analog speaker interface signals, as well as telephone handset/headset interface signals are provided to support functions such as speakerphone mode, telephone emulation, microphone voice record, speaker voice playback, and call progress monitor.

3.3.1 VC Signal Interfaces

Speakerphone Interface

The following signals are supported:

- Speaker Out (M_SPKR_OUT); analog output - Should be used in speakerphone designs where sound quality is important
- Microphone (M_MIC_IN); analog input

Telephone Handset/Headset Interface

The following interface signals are supported:

- Telephone Input (M_LINE_IN), input (TELIN) –Optional connection to a telephone handset interface circuit
- Telephone output (M_LINE_OUTP); output (TELOUT) - Optional connection to a telephone handset interface circuit
- Center Voltage (VC); output reference voltage

HSD Interface

The following interface signals are supported:

- Reset (POR); input
- Sleep (SLEEP); input
- Master Clock (M_CLKIN); input
- Serial Clock (M_SCK); output
- Control (M_CNTRLSIN); input
- Serial Frame Sync (M_STROBE); output
- Serial Transmit Data (M_TXSIN); input
- Serial Receive Data (M_RXOUT); output

3.3.2 VC Interface Signals, Pin Assignments, and Signal Definitions

The VC (20437) 32-pin TQFP hardware interface signals are shown by major interface in Figure 3-5, are shown by pin number in Figure 3-6, and are listed by pin number in Table 3-6.

The VC (20437) hardware interface signals are defined in Table 3-7.

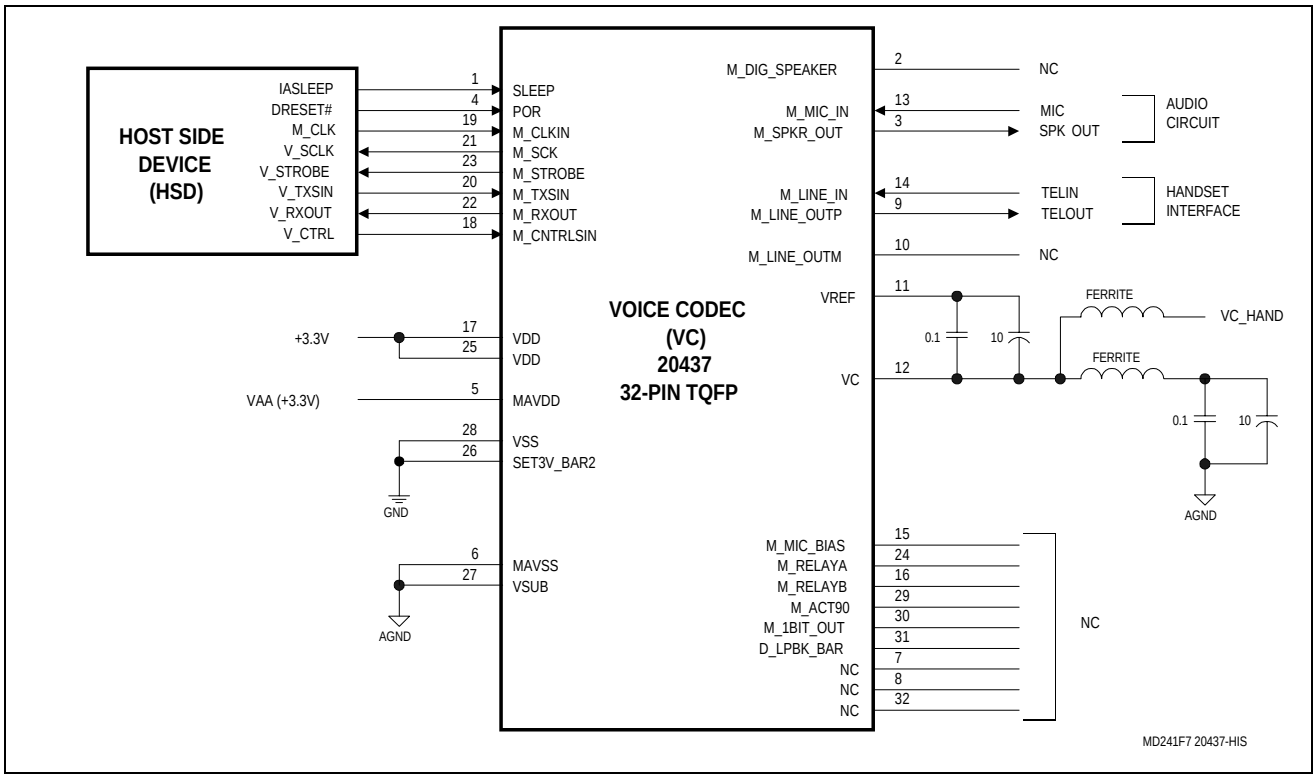

Figure 3-5. VC (20437) 32-Pin TQFP Hardware Interface Signals

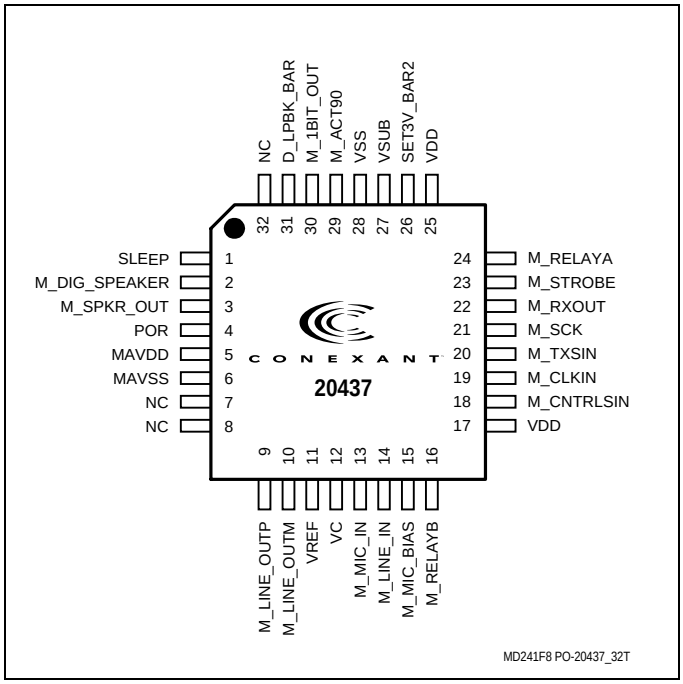

Figure 3-6. VC (20437) 32-Pin TQFP Pin Signals

Table 3-6. VC (20437) 32-Pin TQFP Pin Signals

Pin	Signal Label	I/O	I/O Type	Interface
1	SLEEP	I	Itpd	HSD: IASLEEP
2	M_DIG_SPEAKER	O	Ot2	NC
3	M_SPKR_OUT	O	Oa	Speaker interface circuit
4	POR	I	Itpu	HSD: DRESET#
5	MAVDD		PWR	VAA (+3.3V)
6	MAVSS		AGND	AGND
7	NC			NC
8	NC			NC
9	M_LINE_OUTP (TELOUT)	O	Oa	Handset interface circuit
10	M_LINE_OUTM	O	Oa	NC
11	VREF		REF	VC through capacitors
12	VC		REF	AGND through ferrite bead and capacitors and to and to handset interface circuit (VC_HAND) through ferrite bead
13	M_MIC_IN	I	Ia	Microphone interface circuit
14	M_LINE_IN (TELIN)	I	Ia	Handset interface circuit
15	M_MIC_BIAS			NC
16	M_RELAYB			NC
17	VDD		PWR	+3.3V
18	M_CNTRLSIN	I	Itpd	HSD: V_CTRL
19	M_CLKIN	I	Itpd	HSD: M_CLK
20	M_TXSIN	I	Itpd	HSD: V_TXSIN
21	M_SCK	O	Ot2	HSD: V_SCLK
22	M_RXOUT	O	Ot2	HSD: V_RXOUT
23	M_STROBE	O	Ot2	HSD: V_STROBE
24	M_RELAYA	O	Ot2od	NC
25	VDD		PWR	+3.3V
26	M_SET3V_BAR2	I	Itpu	GND
27	VSUB		AGND	AGND
28	VSS		GND	GND
29	M_ACT90	I	Itpu	NC
30	M_1BIT_OUT	O	Ot2	NC
31	D_LPBK_BAR	I	Itpu	NC
32	NC			NC

Notes:

1. I/O types:

Ia	Analog input
It	Digital input, TTL-compatible
Itpd	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-up
It/Ot2	Digital input, TTL-compatible/digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
It/Ot12	Digital input, TTL-compatible/digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Oa	Analog output
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
AGND	Analog Ground
GND	Digital Ground

See VC (20437) Digital Electrical Characteristics (Table 3-8) and VC (20437) Analog Electrical Characteristics (Table 3-9).

2. Interface Legend:

HSD	Host Side Device

Table 3-7. VC (20437) 32-Pin TQFP Pin Signal Definitions

Label	Pin	I/O Type	Signal Name/Description
SYSTEM SIGNALS			
VDD	17, 25	PWR	**Digital Power Supply.** Connect to +3.3V and digital circuits power supply filter.
MAVDD	5	PWR	**Analog Power Supply.** Connect to +3.3V and analog circuits power supply filter.
VSS	28	GND	**Digital Ground.** Connect to GND.
MAVSS	6	AGND	**Analog Ground.** Connect to AGND.
VSUB	27	GND	**Analog Ground.** Connect to AGND.
POR	4	Itpu	**Power-On Reset.** Active low reset input. Connect to Host RESET#.
SET3V_BAR2	26	Itpu	**Set +3.3V Analog Reference.** Connect to GND.
HSD INTERCONNECT			
SLEEP	1	Itpd	**IA Sleep.** Active high sleep input. Connect to HSD IASLEEP pin.
M_CLKIN	19	Itpd	**Master Clock Input**. Connect to HSD M_CLK pin.
M_SCK	21	Ot2	**Serial Clock Output.** Connect to HSD V_SCLK pin.
M_CNTRL_SIN	18	Itpd	**Control Input.** Connect to HSD V_CTRL pin.
M_STROBE	23	Ot2	**Serial Frame Sync.** Connect to HSD V_STROBE pin.
M_TXSIN	20	Itpd	**Serial Transmit Data.** Connect to HSD V_TXSIN pin.
M_RXOUT	22	Ot2	**Serial Receive Data.** Connect to HSD V_RXOUT pin.
TELEPHONE LINE (DAA)/AUDIO INTERFACE AND REFERENCE VOLTAGE			
M_LINE_OUTP	9	O(DF)	**Telephone Handset Out (TELOUT).** Single-ended analog data output to the telephone handset circuit. The output can drive a 300 Ω load.
M_LINE_IN	14	I(DA)	**Telephone Handset Out (TELIN).** Single-ended analog data input from the telephone handset circuit.
M_MIC_IN	13	I(DA)	**Microphone Input.** Single-ended from the microphone circuit.
M_SPKR_OUT	3	O(DF)	**Modem Speaker Analog Output.** The M_SPKR_OUT analog output reflects the received analog input signal. The M_SPKR_OUT on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the M_SPKR_OUT output is clamped to the voltage at the VC pin. The M_SPKR_OUT output can drive an impedance as low as 300 ohms. In a typical application, the M_SPKR_OUT output is an input to an external LM386 audio power amplifier.
VREF	11	REF	**High Voltage Reference.** Connect to VC through 10 µF and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VREF pin.
VC	12	REF	**Low Voltage Reference.** Connect to analog ground through ferrite bead in series with a parallel combination of 10 µF and 0.1 µF (ceramic). Ensure a very close proximity between these capacitors and VC pin. Use a short path and a wide trace to AGND pin. Also connect to handset interface circuit (VC_HAND) through a ferrite bead.

Table 3-7. VC (20437) 32-Pin TQFP Pin Signal Definitions (Cont'd)

Label	Pin	I/O Type	Signal Name/Description
NOT USED			
M_DIG_SPEAKER	2	Ot2	**Not Used.** Leave open.
M_LINE_OUTM	10	Oa	**Not Used.** Leave open.
M_RELAYA	24	Ot	**Not Used.** Leave open.
M_RELAYB	16	Ot	**Not Used.** Leave open.
M_MIC_BIAS	15	Oa	**Not Used.** Leave open.
M_ACT90	29	Itpu	**Not Used.** Leave open.
M_1BIT_OUT	30	Ot2	**Not Used.** Leave open.
D_LPBK_BAR	31	It	**Not Used.** Leave open.
NC	7, 8, 32	NC	**Internal No Connect.**

Notes:

1. I/O types:

Ia	Analog input
It	Digital input, TTL-compatible
Itpd	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-down
Itpu	Digital input, TTL-compatible, internal 75k ± 25k Ω pull-up
It/Ot2	Digital input, TTL-compatible/digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
It/Ot12	Digital input, TTL-compatible/digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
Oa	Analog output
Ot2	Digital output, TTL-compatible, 2 mA, $Z_{INTERNAL}$ = 120 Ω
Ot12	Digital output, TTL-compatible, 12 mA, $Z_{INTERNAL}$ = 32 Ω
AGND	Analog Ground
GND	Digital Ground

See VC (20437) Digital Electrical Characteristics (Table 3-8) and VC (20437) Analog Electrical Characteristics (Table 3-9).

2. Interface Legend:

HSD	Host Side Device

Table 3-8. VC Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	V_{IN}	-0.30	–	VDD+0.3	V	
Input Voltage Low	V_{IL}	-0.30	–	VDD+0.3	V	
Input Voltage High	V_{IH}	0.4*VDD	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.4	V	
Output Voltage High	V_{OH}	0.8*VDD	–	VDD	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	

Test conditions unless otherwise noted:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF

Table 3-9. VC Analog Electrical Characteristics

Signal Name	Type	Characteristic	Value
M_LINE_IN (TELIN), M_MIC_IN	I (DA)	Input Impedance AC Input Voltage Range Reference Voltage	> 70K Ω 1.1 VP-P +1.35 VDC
M_LINE_OUTP (TELOUT)	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage DC Offset Voltage	300 Ω 0 µF 10 Ω 1.4 VP-P (with reference to ground and a 600 Ω load) +1.35 VDC ± 200 mV
M_SPKR_OUT	O (DF)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage DC Offset Voltage	300 Ω 0.01 µF 10 Ω 1.4 VP-P +1.35 VDC ± 20 mV

Test conditions unless otherwise noted:

1. Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; MAVDD = +3.3 ± 0.3 VDC, TA = 0°C to 70°C

Parameter	Min	Typ	Max	Units
DAC to Line Driver output (600Ω load, 3dB in SCF and CTF) SNR/SDR at:				dB
4Vp-p differential		88/85		
2Vp-p differential		82/95		
-10dBm differential		72/100		
DAC to Speaker Driver output (150Ω load, 3dB in SCF and CTF, -6dB in speaker driver) SNR/SDR at:				dB
2Vp-p		88/75		
1Vp-p		82/80		
-10dBm		72/83		
Line Input to ADC (6dB in AAF) SNR/SDR at –10 dBm		80/95		dB
Input Leakage Current (analog inputs)	-10		10	µA
Output Leakage Current (analog outputs)	-10		10	µA

3.4 ELECTRICAL, ENVIRONMENTAL, AND TIMING SPECIFICATIONS

3.4.1 Operating Conditions and Absolute Maximum Ratings

The operating conditions are specified in Table 3-10.

The absolute maximum ratings are listed in Table 3-11.

Table 3-10. Operating Conditions

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	+3.0 to +3.6	VDC
Operating Temperature Range	T_A	0 to +70	°C

Table 3-11. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +4.0	VDC
Input Voltage	V_{IN}	-0.5 to (VIO +0.5)*	VDC
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (MAVDD + 0.5)	VDC
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VIO +0.5)*	VDC
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	VDC
Latch-up Current (25°C)	I_{TRIG}	±400	mA
* VIO = +3.3V ± 0.3V or +5V ± 5%.			

Caution: Handling CMOS Devices

These devices contain circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage.

An un-terminated input can acquire unpredictable voltages through coupling with stray capacitance and internal cross talk. Both power dissipation and device noise immunity degrades. Therefore, all inputs should be connected to an appropriate supply voltage.

Input signals should never exceed the voltage range from 0.5V or more negative than GND to 0.5V or more positive than VDD. This prevents forward biasing the input protection diodes and possibly entering a latch up mode due to high current transients.

3.4.2 PCI BUS ELECTRICAL, SWITCHING, AND TIMING CHARACTERISTICS

The host bus electrical, switching, and timing characteristics conform to the following specifications:

- PCI Local Bus Specification Version 2.2
- MiniPCI Specification Draft 1.0
- PC Card Standard for CardBus

3.4.3 SERIAL EEPROM INTERFACE TIMING

The serial EEPROM interface timing is listed in Table 3-12 and is shown in Figure 3-7.

Table 3-12. Timing - Serial EEPROM Interface

Symbol	Parameter	Min	Typ.	Max	Units	Test Condition
t_{CSS}	Chip select setup	200 (Note 1)	–	–	ns	
t_{CSH}	Chip select hold	500 (Note 1)	–	–	ns	
t_{DIS}	Data input setup	200 (Note 1)	–	–	ns	
t_{DIH}	Data input hold	1600	–	–	ns	
t_{PD0}	Data input delay	50	–	–	ns	
t_{PD1}	Data input delay	50	–	–	ns	
t_{DF}	Data input disable time	–	–	Note 2	ns	
t_{SV}	Status valid	–	–	Note 3	ns	
t_{SKH}	Clock high	900 (Note 1)	–	–	ns	
t_{SKL}	Clock low	900 (Note 1)	–	–	ns	
–	Endurance	–	10^6	–	Cycles	

Notes:

1. Minimum times for HSD outputs when PCI clock = 33 MHz (times increase with decreasing PCI clock frequency).
2. No requirement.
3. Timing controlled by software for programming of EEPROM. No requirement for EEPROM read into HSD.

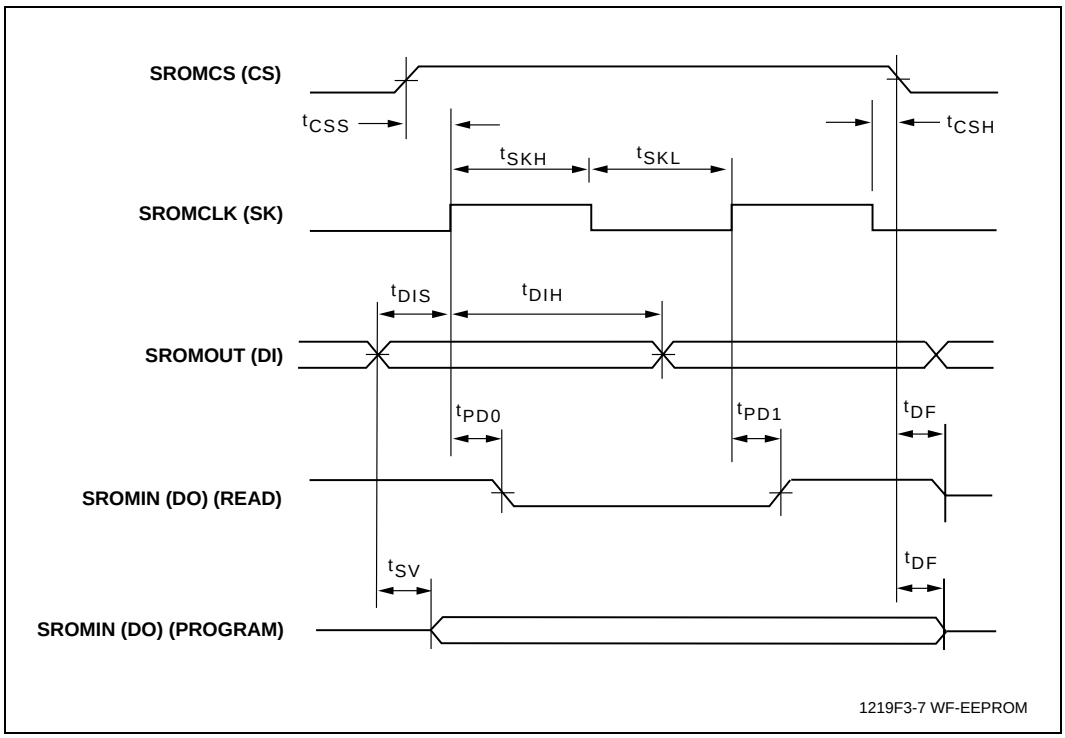

Figure 3-7. Waveforms - Serial EEPROM Interface

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4. CRYSTAL SPECIFICATIONS

Recommended surface-mount crystal specifications are listed in Table 4-1.

Recommended through-hole crystal specifications are listed in Table 4-2.

Table 4-1. Crystal Specifications - Surface Mount

Characteristic	Value
Conexant Part No.	5333R02-020
Electrical	
Frequency	28.224 MHz nom.
Frequency Tolerance	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability	
vs. Temperature	±35 ppm (0°C to 70°C)
vs. Aging	±15 ppm/4 years
Oscillation Mode	Fundamental
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series Resistance, R_1	60 Ω max. @20 nW drive level
Drive Level	100µW correlation; 300µW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C
Mechanical	
Dimensions (L x W x H)	7.5 x 5.2 x 1.3 mm max.
Mounting	SMT
Holder Type	None
Suggested Suppliers	KDS America ILSI America Vectron Technologies, Inc.

Notes

Characteristics @ 25°C unless otherwise noted.

Supplier Information:

KDS America
Fountain Valley, CA 92626
(714) 557-7833

ILSI America
Kirkland, WA 98033
(206) 828 - 4886

Vectron Technologies, Inc.
Lowell, NH 03051
(603) 598-0074

Toyocom U.S.A., Inc.
Costa Mesa, CA
(714) 668-9081

Table 4-2. Crystal Specifications - Through Hole

Characteristic	Value
Conexant Part No.	333R44-011
Electrical	
Frequency	28.224 MHz nom.
Frequency Tolerance	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability	
vs. Temperature	±30 ppm (0°C to 70°C)
vs. Aging	±20 ppm/5 years
Oscillation Mode	Fundamental
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series Resistance, R_1	35 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C
Mechanical	
Dimensions (L x W x H)	11.05 x 4.65 x 13.46 mm max.
Mounting	Through Hole
Holder Type	HC-49/U
Suggested Suppliers	KDS America ILSI America Vectron Technologies, Inc.

Notes

Characteristics @ 25°C unless otherwise noted.

Supplier Information:

KDS America
Fountain Valley, CA 92626
(714) 557-7833

ILSI America
Kirkland, WA 98033
(206) 828 - 4886

Vectron Technologies, Inc.
Lowell, NH 03051
(603) 598-0074

Toyocom U.S.A., Inc.
Costa Mesa, CA
(714) 668-9081

5. LAYOUT GUIDELINES

Good engineering practices must be followed when designing a printed circuit board (PCB) containing the modem and voice codec devices. This is especially important for high performance modem operation with high bit rate data and fax and for high quality voice/audio supporting record/play of analog voice and music, and full-duplex speakerphone operation. Suppression of noise is essential to the proper operation and performance of the modem, DAA, and voice/speakerphone circuits.

Two major aspects of noise in an OEM board design containing the modem device set must be considered:

- On-board generated noise and off-board generated noise that is coupled on-board can affect analog signal levels (especially low levels) and quality as well as affecting analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC) operation. Of particular concern is noise in frequency ranges affecting modem and audio circuit performance.
- On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments. In order to minimize the contribution of the circuit design and PCB layout to EMI, the designer must understand the major sources of EMI and how to reduce EMI to acceptable levels.

Proper PC board layout (component placement and orientation, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to obtain EMI certification.

A board design should also comply with a host interface specification addressing electrical, physical, and environmental requirements.

The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars covering noise suppression techniques are routinely offered by technical and professional associations as well as component suppliers.

These guidelines are offered to help achieve good modem performance, minimize audible noise for audio circuit use, and to minimize EMI generation.

5.1 EMI CONSIDERATIONS

5.1.1 General

1. Because EMI always takes the easiest path to earth ground, ensure that EMI has a good planned path to earth ground. A quiet ground is provided by the case (CardBus)/metallic tabs (MiniPCI), not by the ground pins on the bus. (The ground pins provide effective signal returns to the motherboard, however, at high frequencies these traces become inductors that acquire higher impedance with increasing frequency).
2. Surround noisy signals, especially clocks, with a wide GND guard band. Pay special attention to where the guard bands are grounded, as the effectiveness of this technique will be greatly diminished with increased physical distance from a good ground point.
3. Use multiple vias rather than a single via with power/ground distribution when changing layers on the board. The more vias that are on the board, the lower the impedance.
4. Avoid vias on traces carrying high frequency signals.
5. If radiated emissions move 6 or more dBuV just by slightly moving connected cables, the grounding technique used in design should be improved. At this point, maximize dumping EMI energy directly to the chassis ground without dumping too much EMI energy to scattered ground traces on the board.
6. In a design needing EMI filtering, define an additional "chassis" section adjacent to the case (CardBus)/ tabs (MiniPCI) end of a plug-in card. Most EMI components (usually ferrite beads/capacitor combinations) can be placed in this section. Fill the unused space with a chassis ground plane where possible, and connect it to the case (CardBus)/ tabs (MiniPCI).
7. Keep the current paths of separate board functional areas isolated from each other, thereby limiting the propagation of EMI to all areas of the board. Separate board functional areas include: Digital, DAA, and Analog.
8. Place a series terminating resistor as close as possible to the signal source on clock lines or fast edge rate signals.

5.1.2 Filtering

1. A general rule of thumb is to filter every connector on the board. On modem/audio boards, these filters take the form of ferrite beads and capacitors. Place a ferrite bead in series with the signal and a capacitor between the signal and ground. After the signal is filtered, it must not be exposed to any board noise. Therefore, the filter must be as close to the connector as possible and filtered signals kept away from the digital ground and power.

5.1.3 Decoupling

1. Another way to minimize EMI is to short it to ground through proper decoupling capacitors (caps). Because traces and component leads become inductors at high frequencies, use surface mount caps if possible, and place them close to the device pin being decoupled. Decouple power pins of a device directly to associated ground pins of the device as close to the device as possible - not to a remote ground plane. If you have power and ground planes, connect capacitors to the planes with more than one via. This will decrease the lead inductance and increase the effectiveness of the capacitors.
2. Capacitors can reduce EMI by shorting high frequencies to ground. This is good if the ground plane is properly grounded (i.e., short path to chassis ground). Otherwise, the decoupling caps then need to be used to source as much noise to the ground plane as it can handle. Also, note that the desired value of the decoupling cap depends on the frequency to be eliminated. With higher system clock rates it is necessary to have a mixture of values for decoupling caps (e.g., 0.001 uF, 0.01 uF and 0.1 uF).
3. Sourcing too much energy to ground can be just as harmful to EMI performance as not sourcing enough EMI to ground, if the path to ground is poor. The capacitor value chosen for an offending frequency can be mathematically correct but also cause excessive EMI ripple on the ground. Unless the impedance of ground traces can be reduced, the solution is to reduce the capacitor value. As an example, if the board is excessively radiating at 100 MHz with a 0.01 uF cap, try a 0.047 uF. The idea is to only source as much energy to ground as the ground can handle and no more, or the EMI will radiate.

Capacitor Value	Frequency of Reduced EMI
0.1 uF	10 MHz
0.01 uF	30 MHz
0.001 uF	100 MHz

4. There is some overlap, as these values will change as inductance of the board comes into effect, and the fact you rarely have just one problem frequency. Another rule of thumb, derived from experience, is 0.1 uF for <80 MHz, 0.01 uF for 60-500 MHz, and 0.001 uF for >400 MHz. The designer should provide several different values for de-coupling capacitors. These should be spread evenly around the power pins of devices on the board. A few capacitors can be placed in open areas of the board to stabilize the power and ground.
5. Separate analog power/ground from digital power/ground with inductors or ferrite beads. The side effect of this separation is that the analog circuit cannot dump their high frequency noise to the chassis ground. The EMI characteristic of boards can be improved by using adequate decoupling and by limiting the areas of analog power/ground.
6. The de-coupler on the PCICLK guard band should be 0.001 uF to handle the clock harmonics. Decouple this guard band directly to a VCC pin near the PCICLK pin at the PCI connector.

5.1.4 Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another case. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes in TIP and RING lines replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. Developing two designs in parallel; one based on a 2-layer board and the other based on a 4-layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

5.2 GENERAL LAYOUT GUIDELINES FOR A 2-LAYER PCI BOARD

Follow the guidelines in this section unless otherwise specified by a host bus specification, a local government regulation, or by a specific guideline mentioned in Section 5.3.

5.2.1 Placing Components

1. From the system circuit schematic, identify the digital, analog (for optional voice/speakerphone), and DAA circuits and their components, as well as external signal and power connections. Note the location of pins for power, ground, digital signals, and analog signals for each device.
2. Roughly place digital, DAA, and analog sections on the board.
   a) Place the digital section near the host connector.
   b) Place the DAA section near the telephone line connector.
   c) Place the analog section near the microphone and speaker connectors, when applicable.
3. Place the components starting with the connectors and jacks, then the modem devices (mixed signal devices), and finally the supporting components. Keep the digital and analog components and their corresponding traces as separate as possible and confined to their respective sections on the board.
   a) Allow sufficient clearance around connectors and jacks for mating connectors and plugs.
   b) Allow sufficient clearance around components for power and ground traces.
   c) Allow sufficient clearance around sockets to allow the use of component extractors.
   d) Orient components so pins carrying digital signals extend onto the digital portion of each section and pins carrying analog signals extend onto the analog portion section as much as possible.
   e) Place digital components close together in order to minimize signal trace length.
4. Place digital section components (see specific layout guidelines).
   a) Place the Host Side Device (HSD) near the PCI/MiniPCI/CardBus connector and immediately next to the Digital Isolation Barrier (DIB) with digital signal pins toward host interface connector and power, clock and data pins toward the DIB.
   b) Place host bus interface components close to the host connector in accordance with the applicable bus interface standard or specification.
   c) Place crystal circuits as close as possible to the HSD.
5. Place DAA section components (see specific layout guidelines in Section 5.3.2).
   a) Place the LSD as close to the DIB as possible with analog signal pins toward the telephone line connector and power, clock and data pins toward the DIB.
   b) Place the DIB interface components between the LSD and the DIB.
   c) Place the analog telephone interface components between the LSD and the telephone line connector.
6. Place analog section components optional for voice/speakerphone (see specific layout guidelines).
   a) Place the VC with analog signal pins toward the DAA section and the microphone and speaker, and digital signals toward the HSD.
   b) Place mixed-signal components to straddle the border between analog and digital sections.
   c) Place the analog components close to and on the side of card containing the analog signals.
   d) Avoid placing noisy components and traces near these analog signal traces.
7. Place decoupling (bypass) capacitors close to the pins (usually power and ground) of the device or connector they are decoupling. Make the smallest loop area possible between the capacitor and power/ground pins to reduce EMI. Evenly distribute the decoupling capacitors around the associated device or connector.
8. Provide a "connector" component, usually a zero ohm resistor or a ferrite bead at one point on the PCB to connect one section's ground to another. Allow other points for grounds to be connected together if necessary for EMI suppression.

5.2.2 Power

1. Identify digital power (VDD) and analog power (AVDD) supply connections.
2. Place a 10 µF electrolytic or tantalum capacitor in parallel with a ceramic 0.1 µF capacitor between power and ground at a few points in the digital section. Place one set nearest to where power enters the PCB (edge connector or power connector) and place another set at the furthest distance from where power is supplied to the PCB. These capacitors help to supply current surge demands by the digital circuits and prevent those surges from generating noise on the power lines that may affect other circuits.
3. Generally, route all power traces before signal traces.

5.2.3 Grounds

1. Provide a digital ground plane.
   a) Provide a digital ground plane on the board bottom everywhere except under the DAA section and where the analog ground plane is provided.
   b) Connect the digital ground plane to the case (CardBus)/ tabs (MiniPCI) (chassis ground).
   c) Provide digital ground fill, or islands, in unused space in the digital sections on top the board.
   d) Connect digital ground fill to the digital ground plane using multiple vias and to the case/tabs via multiple traces if possible.
   a) Provide digital ground guard bands around critical traces.
   a) Connect digital ground guard bands to the digital ground plane by one or more vias.
2. Provide separate and isolated DAA digital and DAA analog ground planes in the DAA section.
   a) Provide a DAA analog ground (AGND_LSD) on the board bottom under the DAA analog components.
   b) Provide a DAA digital ground (GND_LSD) on the board bottom side under the DAA digital components.
   c) Provide DAA digital ground fill in unused space around digital components in the DAA section on the top the board. Ensure that this fill is at least 40 mils from any "hot" DAA signal coming from the telephone line connector.
   d) Connect DAA analog ground (LSD_AGND) and DAA digital ground (LSD_GND) together at one point within the DAA, i.e., near the LSD AGND (pin 23) and power capacitor.
3. Provide an analog ground plane in the analog (voice/speakerphone) section.
   a) Provide analog ground plane on the board bottom under the analog section.
   b) Provide analog ground fill in unused space around analog components in the analog section on top the board. Ensure that this fill is at least 40 mils from any "hot" DAA signal coming from the telephone line connector.
   c) Connect the analog and digital ground planes together at a single point, preferably near the case (CardBus)/ tabs (MiniPCI).

5.2.4 Trace Widths

1. Minimize trace width variation on a given trace.
2. Provide 25 mil minimum width for power, ground, and critical signal traces.
3. Provide 15 mil minimum width for crystal traces.
4. Provide 10 mil (preferably 12 - 15 mil) minimum width for analog signal traces (e.g., the M_MIC_IN, M_LINE_OUT, M_LINE_IN, M_SPKR_OUT, VC, and VREF).
5. Provide 5 mil (preferably 10 mil) minimum width for all other traces.

5.2.5 Trace Spacing

1. Provide 15 to 40 mil minimum spacing between analog and digital ground traces.
2. Provide 40 mil minimum spacing around TIP and RING signal traces from the telephone line connector to the first resistor, then normal spacing after the resistor.
3. Provide 40 mil minimum spacing from BR2+ to the first resistor, then normal spacing after the resistor.
4. Provide 10 mil minimum spacing for all analog signals.

5. Provide 8 mil minimum spacing for all digital signals.

5.2.6 Trace Routing

1. Provide consistent trace routing. EMI radiation will occur every time a trace changes impedance, so avoid vias and try to keep a constant trace width for any given signal.
2. Keep high-speed digital traces as short as possible.
3. Keep sensitive analog traces as short as possible.
4. Provide maximum isolation between traces carrying noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, separate noise source traces and noise sensitive traces with traces carrying neutral signals.
5. Keep digital signals within the digital section and analog signals within the analog section (placement of isolation traces should prevent these traces from straying outside their respective section).
6. Route digital traces perpendicular to analog traces to minimize signal cross coupling.
7. Provide isolation traces (usually ground traces) to ensure that analog signals are confined to the analog section and digital traces remain out of the analog section. A trace may have to be narrowed to route it though a mixed analog/digital IC, but try to keep the trace continuous.
    a. Route an analog isolation ground trace or fill, at least 50 mil to 100 mil wide, around the border of the analog section; put on both sides of the PCB.
    b. Route a digital isolation ground trace or fill, at least 50 mil to 100 mil wide, and 200 mil wide on one side of the PCB edge, around the border of the digital section.
8. Route the traces between components by the shortest possible path.
9. Route the traces between bypass capacitors to IC pins, at least 25 mil wide; avoid vias if possible.
10. Gather signals that pass between sections (typically low speed control and status signals) together and route them between sections through a path in the isolation ground traces at one (preferred) or two points only. If the path is made on one side only, then the isolation trace can be kept contiguous by briefly passing it to the other side of the PCB to jump over the signal traces.
11. Provide rounded or 45 degree corners. Avoid right angle (90 degree) turns on high frequency traces.
12. Minimize the number of through-hole connections (feedthroughs/vias) on traces carrying high frequency signals.
13. Keep all signal traces away from crystal circuits.
14. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.
15. Provide adequate clearance (e.g., 60 mil minimum) around feedthroughs in any internal planes in the DAA circuit.
16. Eliminate ground loops, which are unexpected current return paths to the power source.

5.3 SPECIFIC LAYOUT GUIDELINES FOR A 6-LAYER MINI PCI BOARD

This section describes layout guidelines specifically for a 6-layer data/fax card. Components identified in this section refer to a SmartDAA-based reference design schematic.

For a MiniPCI card, follow design guidelines documented in the MiniPCI Specification.

5.3.1 Digital Section

Crystal Circuit

1. Place the two bypass capacitors, the series output resistor and the amplifier feedback resistor as close as possible to the HSD crystal pins to reduce induced noise levels and minimize any parasitic inductance and capacitance which could affect the crystal oscillator (Figure 5-2). **Note: PCB layout of the crystal circuit is extremely critical; undesired parasitics due to poor layout may cause circuit instability preventing proper crystal circuit startup.**
2. Keep the traces to the HSD crystal pins, SDXTAL1 (pin 74) and SDXTAL2 (pin 75), extremely short with no bend greater than 45 degrees and containing no vias (Figure 5-2).
3. Place digital ground fill under the crystal on top the board extending approximately 40 mils beyond the crystal case area. Do not put digital ground under the crystal case in the digital ground plane on the bottom of the board.
4. Connect the bypass capacitors directly to the digital ground fill.

DIB Interface

1. Place and rotate the HSD close to the PCI connector and to the DIB to minimize trace length of PCI and DIB signals.
2. Place the DIB transformer and DIB capacitors over the 110-mil (minimum gap = 2.7 mm = 106.3 mil) DAA isolation gap with the transformer closest to the HSD such that the PWRCLKP, PWRCLKN, DIB_DATAP, and DIB_DATAN traces can be routed with no more than one 90° turn rounded at no more than 45° angle, and without vias. **Note: The PWRCLKP and PWRCLKN signals generate noise and the trace routing is extremely critical. The PWRCLKP and PWRCLKN traces must be extremely short, at least 10 mil wide, and be surrounded by GND guard band. Minimize the area used by the PWRCLKP and PWRCLKN traces.**

MiniPCI Signal Routing

1. Layout PCI traces in accordance with the MiniPCI Local Bus Specification Version 1.0.
2. Route the PCI interface signals directly to the PCI connector. The HSD pinouts are arranged such that signals can be routed to the PCI connector with only one via if needed. If any signals cross, the net-list is wrong. The essential rules are: consistent trace aperture, minimum number of vias, trace bends at 45 degree angle maximum.
4. Provide 15-mil minimum trace width for the PCICLK clock signal. Keep the trace width as consistent as possible to minimize impedance change. The clocks should always be routed on the top of the board.
5. The MiniPCI specification puts a strict length limit on PCI signals. The PCICLK trace must be 1.0 ± 0.1" in length. The reference design achieves the required length by performing a zigzag routing with (a) rounded corners for lower EMI and (b) approximately double-width traces compared to other PCI interface signals for lower impedance/EMI (Figure 5-1).
6. The PCICLK signal is one of the largest sources of EMI on PCI peripheral designs. Surround this trace on both sides by GND guard bands along the entire length of PCICLK. This technique also approximates the required impedance relationship of PCICLK with respect to ground distribution. Connect this guard band to GND pins immediately next to the PCICLK pin at the PCI connector.

5.3.2 DAA Section

Note: A DAA is governed by local government regulations covering subjects such as component spacing, high voltage suppression, and current limiting.

DAA Isolation Gap

1. Provide a 110-mil gap (no traces within the gap) around the DAA section on the top and bottom of the board with the gap positioned directly under the DIB transformer and DIB capacitors.

DAA Section Grounding

1. Provide separate and isolated digital and analog areas in the DAA section.
2. Provide an isolated DAA analog ground plane (LSD_AGND) on the bottom of the board underneath the analog circuits and extending to the 110-mil gap on three sides and to midway underneath the LSD. **Do not provide a LSD_AGND plane on top of the board due to space restrictions. Leave analog components on top separated by gaps.**
3. Provide an isolated DAA digital ground plane (LSD_GND) on the bottom of the board underneath the digital components and extending to the 110-mil gap on three sides and to midway underneath the LSD. Place an LSD_GND plane on the top of the board, i.e., LSD_GND islands around components, and extending to the 110-mil gap on three sides and to midway underneath the LSD. Connect the top and bottom LSD_GND planes in several places with vias.
4. Connect to LSD_AGND and LSD_GND planes together at one tie point (U8) near AGND (pin 23) and GND (DGND).
5. Route separate traces from C28 to AVDD (pin 24) and from C28 to DVDD (Pin 26) to minimize noise coupling.
6. Route a single trace from C28 to C30.
7. Route a single trace from C28 to U8 (Ground Tie) then to AGND (pin 23).
8. All components connections to AGND should be to the AGND_LSD ground plane by a via.

DIB Interface

1. Place the LSD within the DAA section such that the LSD side with analog signals (pins 9-16) is oriented toward the analog circuits, and the LSD side with digital signals (pins 25-32) is oriented toward the DIB. This should allow the DIB signals traces to be routed to components and to the LSD without vias.
2. Route the DIB power and clock signals from the DIB to the connecting diode and capacitors and then to the LSD with **extremely** short traces without vias. Try to keep all the components in the path of a straight trace.
3. Route the DIB data signals from the DIB to the connecting resistors and then to the LSD with short traces without vias.

DC Hold and Impedance Match Interface

1. Place the components connecting to RXI (pin 3) extremely close to the RXI pin.
2. Place Q6 close to TXF (pin 19) and TXO (pin 20), with TXF (pin 19) having priority.
3. Provide isolated heat sink planes on the top and bottom of the board for Q4 collector. Each plane area should be as large as possible (at least the width and twice the length of Q4). Connect the heat sink planes with no less than nine vias. Solder the Q4 tab (collector) to the top plane.

Diode Bridge

1. Route a 40-mil minimum trace directly from BR + to the Q4 collector (Figure 5-4).
2. Route a 14-mil trace from thick trace to R6, C10 and C12 (Figure 5-4).
3. Provide 40-mil spacing around the trace from BR2+ to the first resistor, then normal spacing after the resistor.
4. Connect the MOV between BR2+ and BR2-

VC and VREF Circuit

5. Place C42 extremely close to VREF (pin 8) and VC (pin 7) and place C44 immediately next to C42.
6. Route a single extremely short trace from C42 to VREF (pin 8).
7. Route a single, short, straight trace from VC (pin 7) to the common nodes of C42 and C44.
8. Route an extremely short trace from C44 to a via connected to AGND_LSD.

Telephone Line Interface

9. Connect the 1000 pF 2 KV capacitor to Telephone Line TIP to chassis GND across the 110-mil gap immediately next to the RJ-11 plug.
10. Connect the 1000 pF 2 KV capacitor to Telephone Line RING to chassis GND across the 110-mil gap immediately next to the RJ-11 plug.
11. Provide 25-30 mil traces for the TIP and RING traces.

12. Provide 40-mil spacing around traces from TIP and RING at the RJ-11 plug to BR2 and the first resistor, then normal spacing after the resistor.
13. Provide 10 mil spacing minimum for other analog signal traces.
14. Minimize the number of signal traces on the bottom of the board.

Handset Interface (Optional)

1. Connect the 1000 pF 2 KV capacitor to Handset TIP to chassis GND across the 110-mil gap immediately next to the RJ-11 plug.
2. Connect the 1000 pF 2 KV capacitor to Handset RING to chassis GND across the 110-mil gap immediately next to the RJ-11 plug.
3. Position the voice relay and handset pickup detector with the DAA section.

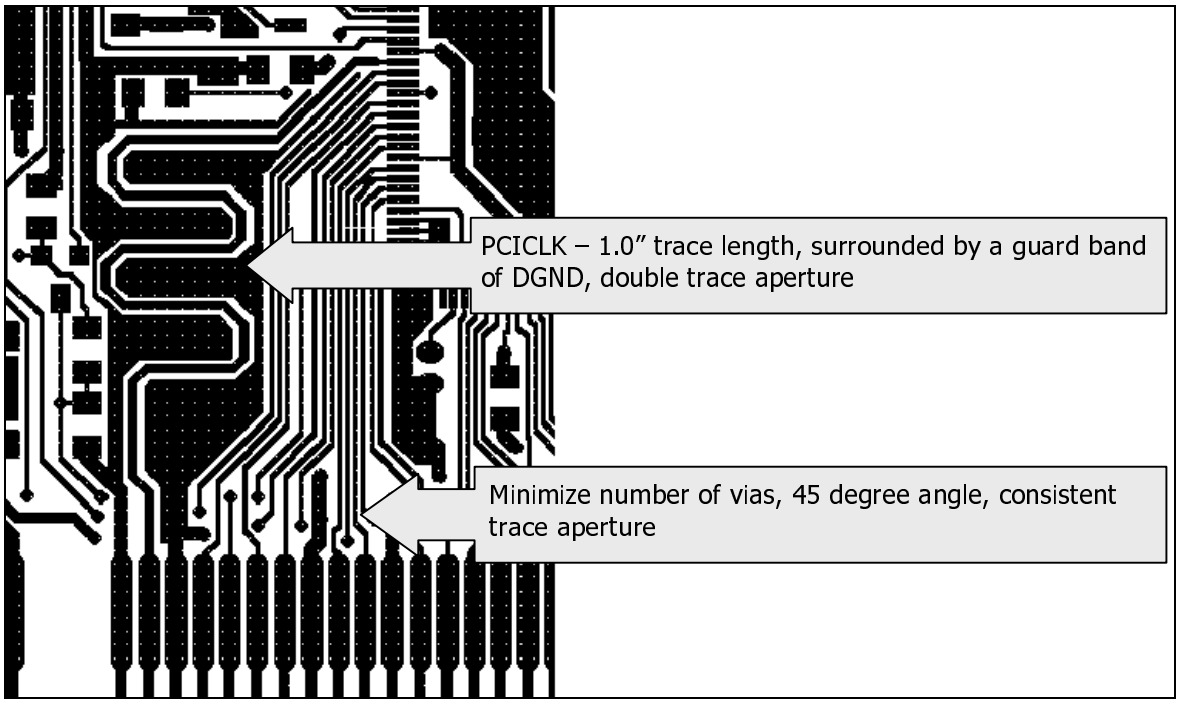


Figure 5-1. PCICLK Guard Band Technique

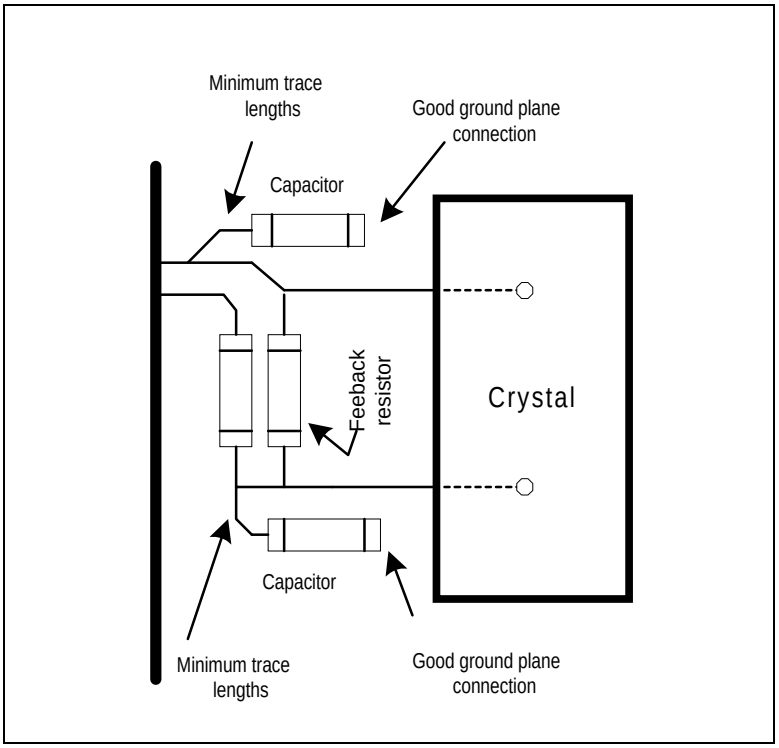


Figure 5-2. Crystal Solution

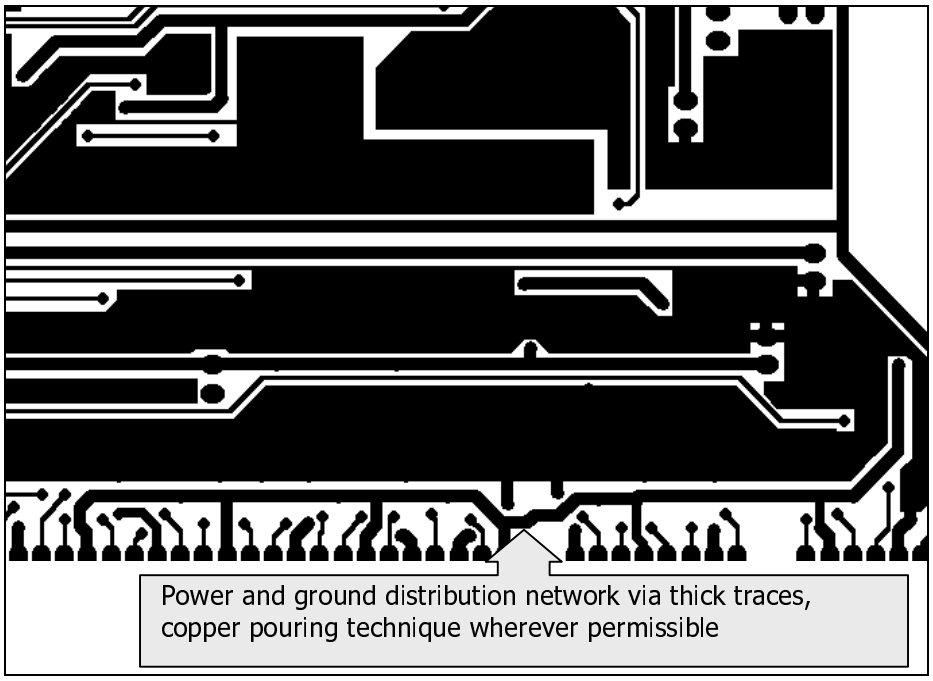


Figure 5-3. Power and Ground Distribution

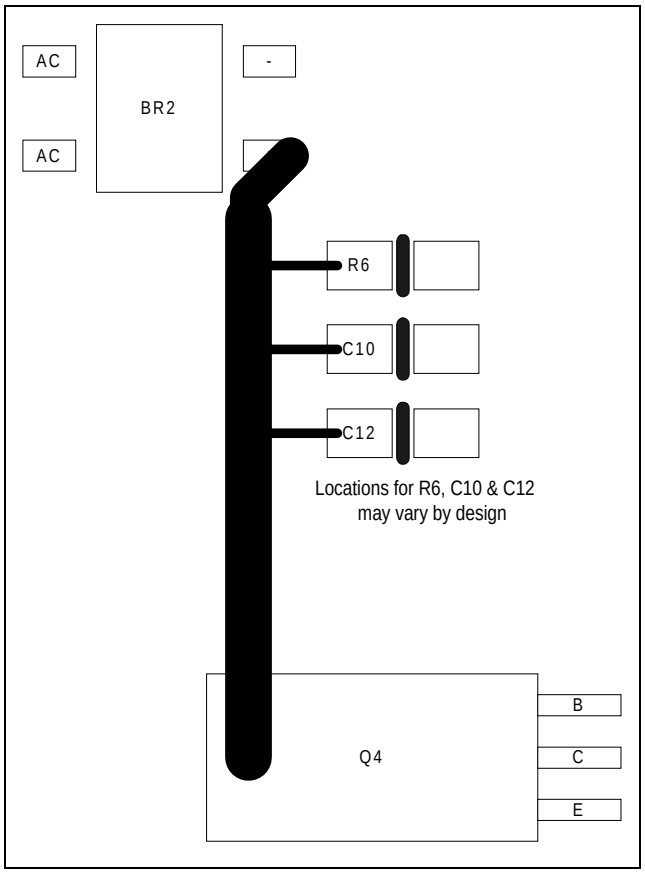


Figure 5-4. Bridge Connections

5.4 PACKAGE DIMENSIONS

The 100-pin TQFP package dimensions are shown in Figure 5-5.

The 32-pin TQFP package dimensions are shown in Figure 5-6.

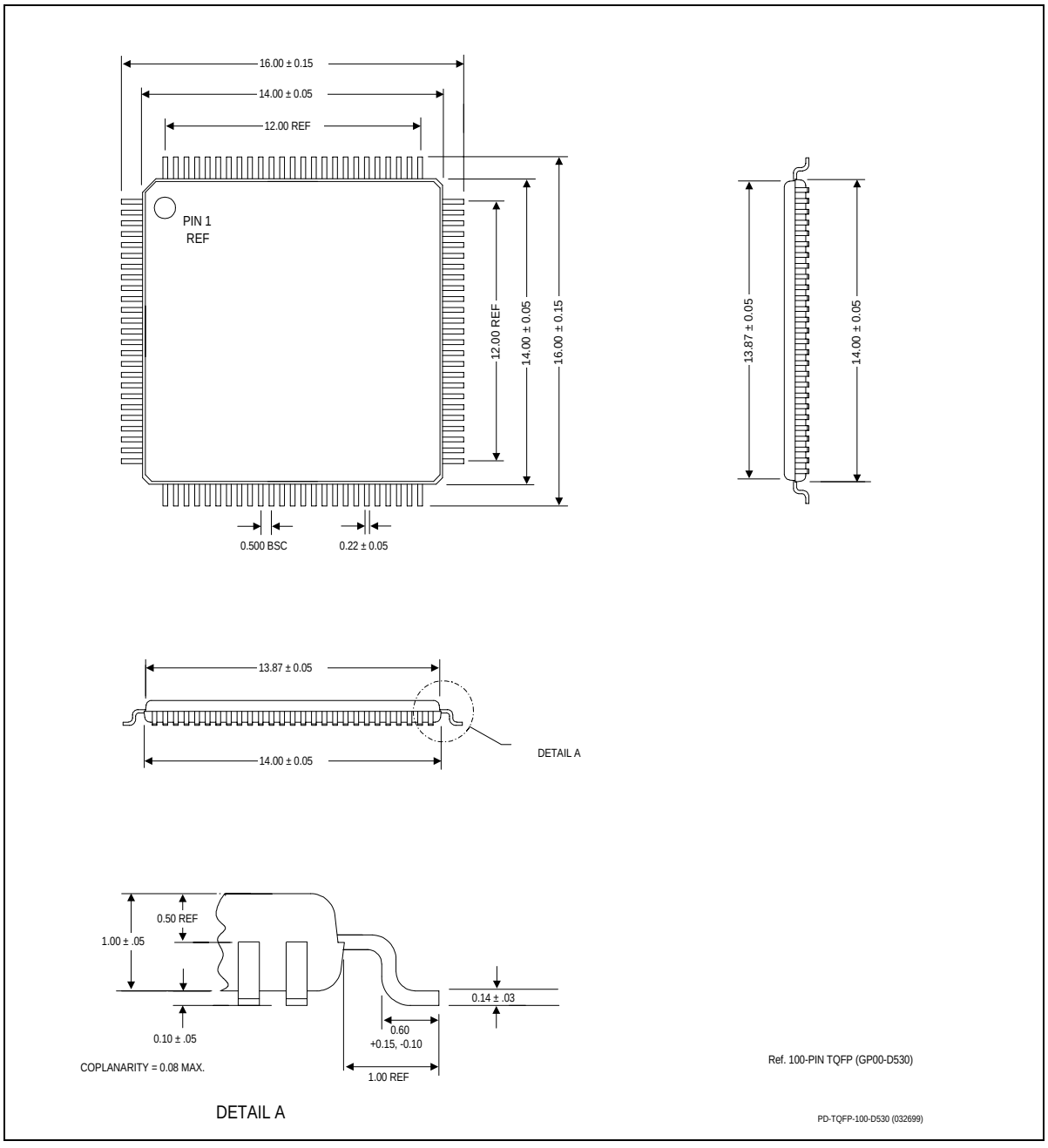
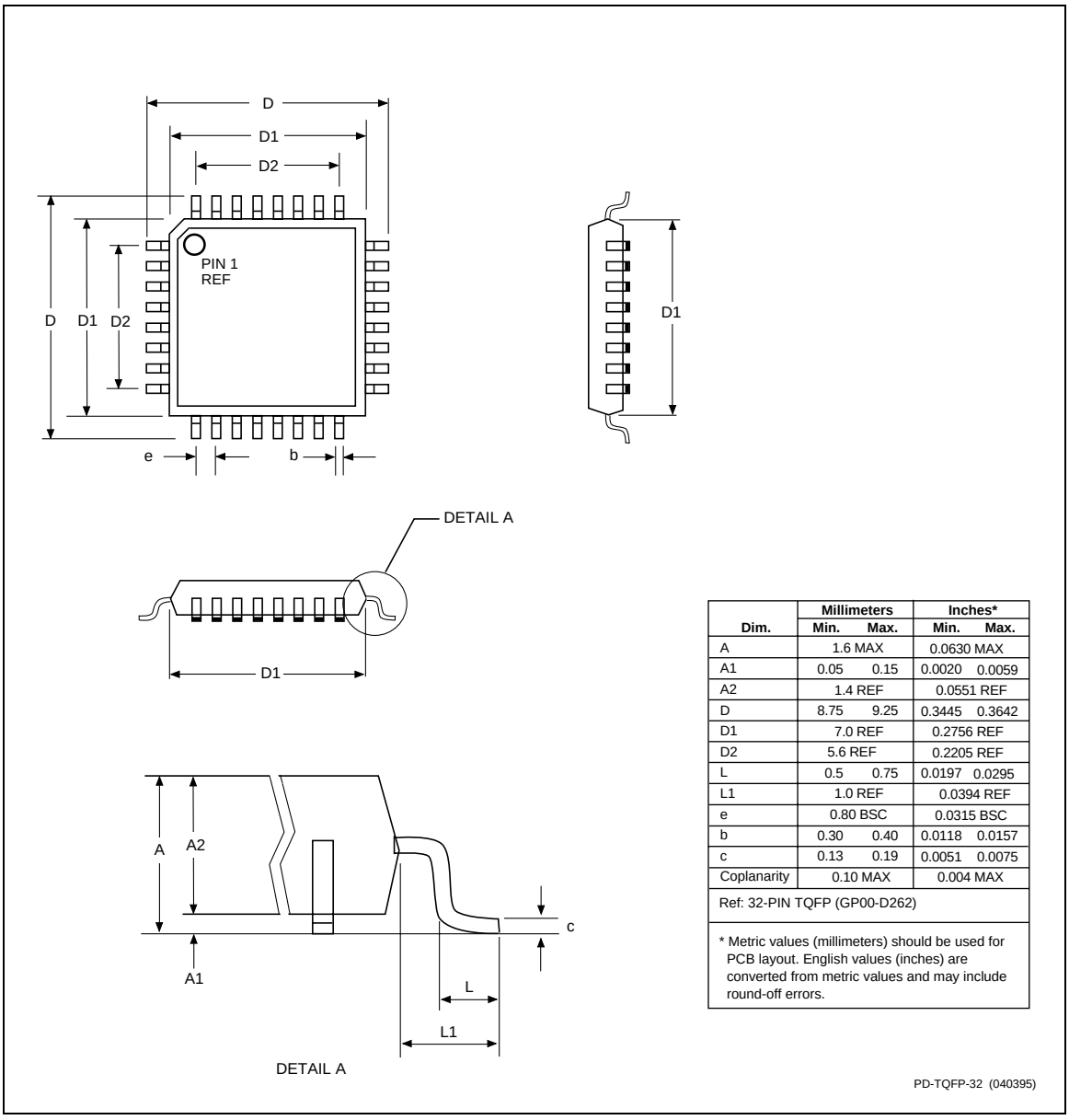


Figure 5-5. Package Dimensions - 100-Pin TQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	7.0 REF		0.2756 REF	
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 5-6. Package Dimensions - 32-pin TQFP

6. HOST SOFTWARE INTERFACE

6.1 PCI CONFIGURATION REGISTERS

The PCI Configuration registers are located in the HSD. Table 6-1 identifies the configuration register contents that are supported in the HSD:

Table 6-1. PCI Configuration Registers

Offset (Hex)	Bit 31:24	Bit 23:16	Bit 15:8	Bit 7:0
00	Device ID		Vendor ID	
04	Status (see Table 6-2)		Command (see Table 6-3)	
08	Class Code			Revision ID
0C	Not Implemented	Header Type	Latency Timer	Not Implemented
10	Base Address 0 - Memory (HSD)			
14	Base Address 1 – I/O (Dummy)			
18	Unused Base Address Register			
1C	Unused Base Address Register			
20	Unused Base Address Register			
24	Unused Base Address Register			
28	CIS Pointer (CardBus Only)			
2C	Subsystem ID		Subsystem Vendor ID	
30	Not Implemented			
34	Reserved			Cap Ptr
38	Reserved			
3C	Max Latency	Min Grant	Interrupt Pin	Interrupt Line
40	Power Management Capabilities (PMC) (see Table 6-4)		Next Item Ptr = 0	Capability ID =01h
44	Data	PMCSR_BSE = 0 Bridge Support Extensions	Power Management Control/Status Register (PMCSR) (see Table 6-5)	

6.1.1 0x00 - Vendor ID Field

This 16-bit read-only field identifying the device manufacturer is loaded from the serial EEPROM after reset events. The value is 14F1 for Conexant.

6.1.2 0x02 - Device ID Field

This 16-bit read-only field identifying the particular device is loaded from the serial EEPROM after reset events. The default Device ID if serial EEPROM is not loaded is 0x1085.

6.1.3 0x04 - Command Register

Command Register										
15 – 10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	r/w	r/w	0	r/w	0	0	0	r/w	R/w	r/w

r/w indicates the bit is read or write.

The Command Register bits are described in Table 6-2.

Table 6-2. Command Register

Bit	Description
0	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. The bit state is 0 after PCIRST# is deasserted.
1	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. The bit state is 0 after PCIRST# is deasserted.
2	Controls a device's ability to act as a master on the PCI Bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. The bit state is 0 after PCIRST# is deasserted.
5-3	Not Implemented.
6	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device must ignore any parity errors that it detects and continue normal operation. The bit state is 0 after PCIRST# is deasserted.
7	This bit is used to control whether or not a device does address/data stepping. This bit is read only from the PCI interface. It is loaded from the serial EEROM after PCIRST# is deasserted.
8	This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver. The bit state is 0 after PCIRST# is deasserted.
9	This bit controls whether or not a master can do fast back-to-back transactions to different devices. A value of 1 means the master is allowed to generate fast back-to-back transactions to different agents as described in Section 3.4.2 of the PCI 2.1 specification. A value of 0 means fast back-to-back transactions are only allowed to the same agent. The bit state is 0 after PCIRST# is deasserted.
15-10	Reserved

6.1.4 0x06 - Status Register

Status Register Bits											
15	**14**	**13**	**12**	**11**	**10 – 9**	**8**	**7**	**6**	**5**	**4**	**3 - 0**
r/c	r/c	r/c	r/c	r/c	01	r/c	0	0	0	1	0000

r/c indicates the bit is readable and clearable (by writing a '1' to corresponding bit position)

The Status Register bits are described in Table 6-3.

Status register bits may be cleared by writing a '1' in the bit position corresponding to the bit position to be cleared. It is not possible to set a status register bit by writing from the PCI Bus. Writing a '0' has no effect in any bit position.

Table 6-3. Status Register

Bit	Description
3-0	Reserved
4	Extended capabilities = 1.
7-5	Not Implemented.
8	This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command Register) is set.
10-9	These bits encode the timing of DEVSEL#. 01 is supported corresponding to medium speed.
11	Signaled Target Abort. Not implemented.
12	Received Target Abort. This bit must be set by a master device whenever its transaction is terminated with Target-Abort.
13	Received Master Abort. This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort.
14	Signaled System Error. This bit must be set whenever the device asserts SERR#.
15	Detected Parity Error. This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).

6.1.5 0x08 - Revision ID Field

This 8-bit read-only field identifying the device revision number is hardcoded in the device.

6.1.6 0x09 - Class Code Field

This 24-bit field, contains three 8-bit sub-fields. The upper byte is a base class code: 07 indicates a communications controller. The middle byte is a sub-class code: 80 indicates "other" type of device. The lower byte is 00 which indicates no register level programming defined. The value of the entire Class Code field is 0x078000.

6.1.7 0x0D - Latency Timer Register

The Latency Timer register specifies, in units of PCI Bus clocks, the value of the Latency Timer for this PCI Bus master. This register has 5 read/write bits (MSBs) plus 3 bits of hardwired zero (LSBs). The Latency Timer Register is loaded into the PCI Latency counter each time FRAME# is asserted to determine how long the master is allowed to retain control of the PCI Bus. This register is loaded by system software. The default value for Latency Timer is 00.

6.1.8 0x0E - Header Type Field

Hardwired to 00.

6.1.9 0x28 - CIS Pointer Register

This register points to the CIS memory located in the HSD's memory space.

6.1.10 0x2C - Subsystem Vendor ID Register

Subsystem Vendor ID register is supported. Loaded from the serial EEPROM after PCIRST# is deasserted.

6.1.11 0x2E- Subsystem ID Register

Subsystem ID register is supported. Loaded from the serial EEPROM after PCIRST# is deasserted.

6.1.12 0x34 - Cap Ptr

Capabilities Pointer (CAP_PTR) at offset 0x34 containing hardcoded value 0x40.

6.1.13 0x3C - Interrupt Line Register

The Interrupt Line register is a read/write 8-bit register. POST software will write the value of this register as it initializes and configures the system. The value in this register indicates which of the system interrupt controllers the device's interrupt pin is connected to.

6.1.14 0x3D - Interrupt Pin Register

The Interrupt Pin register tells which interrupt pin the device uses. The value of this register is 0x01, indicating that INTA# will be used.

6.1.15 0x3E - Min Grant Register

The Min Grant register is used to specify the devices desired settings for Latency Timer values. The value specifies a period of time in units of 0.25 microsecond. Min Grant is used for specifying the desired burst period assuming a 33 MHz clock. This register is loaded from the serial EEPROM after PCIRST# is deasserted.

6.1.16 0x3F - Max Latency Register

The Max Latency register is used to specify the devices desired settings for Latency Timer values. The value specifies a period of time in units of 0.25 microsecond. Min Latency specifies how often the device needs to gain access to the PCI Bus. This register is loaded from the serial EEPROM after PCIRST# is deasserted.

6.1.17 0x40 - Capability Identifier

The Capability Identifier is set to 01h to indicate that the data structure currently being pointed to is the PCI Power Management data structure.

6.1.18 0x41 - Next Item Pointer

The Next Item Pointer register describes the location of the next item in the function's capability list. The value given is an offset into the function's PCI Configuration Space. The value of 00h indicates there are no additional items in the capabilities list.

6.1.19 0x42 - PMC - Power Management Capabilities

The HSD contains power management as described in the PCI Power Management Specification, Revision 1.0 Draft, dated Mar 18, 1997.

The HSD Configuration registers include the following Power Management features:

- Status register bit 4 set to 1 to indicate support for New Capabilities
- Capabilities Pointer (CAP_PTR) at offset 0x34 containing hardcoded value 0x40
- Power Management Register block at offset 0x40 and 0x44 (see Table 6-1)

The Power Management Capabilities register is a 16-bit read-only register which provides information on the capabilities of the function related to power management (Table 6-4).

Table 6-4. Power Management Capabilities (PMC) Register

Bit	R/W	Description
2:0	R	Version. 010b indicates compliance with Revision 1.0 of the *PCI Power Management Interface Specification.*
3	R	PME Clock. Hard coded to 0 to indicate that the PCI clock is **not** required for PME generation.
4	R	Reserved (= 0).
5	R	DSI (Device Specific Initialization). Loaded from serial EEPROM.
8:6	R	Aux. Current. Loaded from serial EEPROM.
9	R	D1_Support. When set to a 1, the HSD device supports D1 power state (loaded from serial EEPROM).
10	R	D2_ Support. When set to a 1, the HSD device supports D2 power state (loaded from serial EEPROM).
15:11	R	These 5 bits indicate which power states allow assertion of PME (loaded from serial EEPROM). A value of 0 for any bit indicates that the function cannot assert the PME# signal while in that power state. Bit 11: 1 = PME# can be asserted from D0 Bit 12: 1 = PME# can be asserted from D1 Bit 13: 1 = PME# can be asserted from D2 Bit 14: 1 = PME# can be asserted from D3hot Bit 15: 1 = PME# can be asserted from D3cold.

6.1.20 0x44 - PMCSR - Power Management Control/Status Register (Offset = 4)

This 16-bit register is used to manage the PCI function's power management state as well as to enable/monitor power management events (Table 6-5).

Table 6-5. Power Management Control/Status Register (PMCSR)

Bit	R/W	Description
1:0	R/W	Power State. 00 = D0 01 = D1 10 = D2 11 = D3.
7:2	R	Reserved (= 000000b).
8	R/W	PME_En. A 1 enables PME assertion.
12:9	R/W	Data_Select. Selects Data and Data Scale fields.
14:13	R	Data Scale. Associated with Data field. Loaded from serial EEPROM.
15:11	R/C	PME_Status. This bit is sticky when PME assertion from D3_cold is supported. PME_Status = 1 indicates PME asserted by the HSD device. Writing 1 clears PME_Status. Writing 0 has no effect.
R: Bit(s) is (are) read only. R/W: Bit(s) is (are) readable and writeable. R/C: Bit(s) is (are) readable, and clearable by writing 1 (bit may not be set by writing).		

6.1.21 0x46 - PMCSR_BSE - PMCSR PCI to PCI Bridge Support Extensions

PMCSR_BSE is cleared to 0 to indicate that bus power/clock control policies have been disabled.

6.1.22 0x47 - Data

This register is used to report the state dependent data requested by the Data_Select field. The value of this register is scaled by the value reported by the Data_Scale field.

6.2 BASE ADDRESS REGISTER

HSD provides a single Base Address Register. The Base Address Register is a 32 bit register that is used to access the HSD register set. Bits 3:0 are hard-wired to 0 to indicate memory space. Bits 15-4 will be hard-wired to 0. The remaining bits (31 - 16) will be read/write. This specifies that this device requires a 64k byte address space. After reset, the Base Address Register contains 0x00000000.

The 64k byte address space used by the HSD is divided into 4k-byte regions. Each 4k-byte region is used as Table 6-6.

Table 6-6. HSD Address Map

Address [15:12]	Address [11:0]	Region Name	Description
0x0	0x0-0xfff	BASIC2 Registers	Buffers, control, and status registers
0x1	0x0-0xfff	CIS Memory	Data loaded from Serial EEPROM for Card Bus applications
0x2	0x0-0xfff	DSP Scratch Pad	Access to DSP scratch pad registers
0x3	0x0-0xfff	Reserved	
0x4	0x0-0xfff	Reserved	
0x5-0xF	0x0-0xfff	Reserved.	

6.3 SERIAL EEPROM INTERFACE

The PCI Configuration Space Header and Power Management registers customizable fields are loaded from EEPROM during Power On Reset and during D3 to D0 power transition soft reset. If the EEPROM is missing, default hard-coded values are used. This section describes how the EEPROM content maps into the registers. The PCI Configuration Space Header and Power Management information is used by the PC BIOS/Windows OS to find the driver for this board and also to find out the extent PCI Power Management is typically supported on the modem board.

Obtain the appropriate EEPROM.TXT file (unique to each software configuration) from the local Conexant sales office.

6.3.1 Supported EEPROM Sizes

Two EEPROM sizes are supported: 256 by 16 bit (e.g., 93LC66B) as shown in Table 6-7 and 128 by 16 bit (e.g., 93LC56B) as shown in Table 6-8. The difference is the 256-word version supports modem default country selection from the EEPROM and also supports CardBus designs, whereas the 128-word version supports neither.

The EEPROM text file used by the DOS4GW B2EPROM program utility lists the EEPROM content 8 bits per line in hexadecimal format. The least significant 8 bits are listed first followed by the most significant 8 bits of the 16-bit word.

Table 6-7. EEPROM Content for 256 Words by 16 Bits per Word

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	Device ID															
01	Vendor ID															
02	Subsystem Device ID															
03	Subsystem Vendor ID															
04	Max_Lat								Min_Gnt							
05	Don't Care				PMC bit 8	PMC bit 7	PMC bit 6	PME DRV	Class Code							
06	Sub-Class Code								Prog. I/F							
07	CardBus CIS Pointer High															
08	CardBus CIS Pointer Low															
09	D0C		D1C		D2C		D3C		D0D		D1D		D2D		D3D	
0A	D3 power consumed								D2 power consumed							
0B	D1 power consumed								D0 power consumed							
0C	D3 power dissipated								D2 power dissipated							
0D	D1 power dissipated								D0 power dissipated							
0E	D3_ Cold	D3_ Hot	D2	D1	D0	D2_ State	D1_ State	DSI	Load CISRAM Count							
0F-FE	Don't Care								Don't Care							
FF	Don't Care								Don't Care							

Table 6-8. EEPROM Content for 128 Words by 16 Bits per Word

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	Device ID															
01	Vendor ID															
02	Subsystem Device ID															
03	Subsystem Vendor ID															
04	Max_Lat								Min_Gnt							
05	Don't Care				PMC bit 8	PMC bit 7	PMC bit 6	PME DRV	Class Code							
06	Sub-Class Code								Prog. I/F							
07	CardBus CIS Pointer High															
08	CardBus CIS Pointer Low															
09	D0C		D1C		D2C		D3C		D0D		D1D		D2D		D3D	
0A	D3 power consumed								D2 power consumed							
0B	D1 power consumed								D0 power consumed							
0C	D3 power dissipated								D2 power dissipated							
0D	D1 power dissipated								D0 power dissipated							
0E	D3_ Cold	D3_ Hot	D2	D1	D0	D2_ State	D1_ State	DSI	Load CISRAM Count							
0F-7F	Don't Care								Don't Care							

6.3.2 Definitions

Device ID Register

This mandatory 16-bit register identifies the type of device and is assigned by Conexant. Valid values are:

Modem-Interface	Modem Part Number	Device ID	Comments
SmartHCF/M-PCI	P9573-11 + 20463-12	1463	Data/Fax
SmartHCF/M-PCI	P9573-11 + 20463-12	1464	Data/Fax/Remote TAM
SmartHCF/MS-PCI	P9573-11 + 20463-12 + 20437-11	1465	Data/Fax/Voice/Speakerphone
SmartHCF/MS-PCI	P9573-11 + 20463-12 + 20437-11	1466	Full-Featured minus Handset
SmartHCF/MW-PCI	P9573-11 + 20463-11	1453	Data/Fax
SmartHCF/MW-PCI	P9573-11 + 20463-11	1454	Data/Fax/Remote TAM
SmartHCF/MWS-PCI	P9573-11 + 20463-11 + 20437-11	1455	Data/Fax/Voice/Speakerphone
SmartHCF/MWS-PCI	P9573-11 + 20463-11 + 20437-11	1456	Full-Featured minus Handset
SmartHCF/M-CB	P9573-21 + 20463-12	1363	Data/Fax
SmartHCF/M-CB	P9573-21 + 20463-12	1364	Data/Fax/Remote TAM
SmartHCF/MS-CB	P9573-21 + 20463-12 + 20437-11	1365	Data/Fax/Voice/Speakerphone
SmartHCF/MS-CB	P9573-21 + 20463-12 + 20437-11	1366	Full-Featured minus Handset
SmartHCF/MW-CB	P9573-21 + 20463-11	1353	Data/Fax
SmartHCF/MW-CB	P9573-21 + 20463-11	1354	Data/Fax/Remote TAM
SmartHCF/MWS-CB	P9573-21 + 20463-11 + 20437-11	1355	Data/Fax/Voice/Speakerphone
SmartHCF/MWS-CB	P9573-21 + 20463-11 + 20437-11	1356	Full-Featured minus Handset

Vendor ID Register

This mandatory 16-bit register identifies the manufacturer of the device. The value in this read-only register is assigned by a central authority (i.e., the PCI SIG) that controls the issuance of the numbers. The value is 14F1 for Conexant.

Subsystem Vendor ID and Subsystem Device Register

The subsystem vendor ID is obtained from the SIG, while the vendor supplies its own subsystem device ID. These values are supplied by OEM. Until these values are assigned, Conexant uses default values for Subsystem Vendor ID and Subsystem Device ID which are the same as Vendor ID and Device ID, respectively.

A PCI functional device may be contained on a card or be embedded within a subsystem. Two cards or subsystems that use the same PCI functional device core logic would have the same vendor and device IDs. These two optional registers are used to uniquely identify the add-in card or subsystem that the functional device resides within. Software can then distinguish the difference between cards or subsystems manufactured by different vendors but with the same PCI functional device on the card or subsystem. A value of zero in these registers indicates that there isn't a subsystem vendor and subsystem ID associated with the device.

Min_Gnt Register

This register is assigned by Conexant. The value is 00.

This register is optional for a bus master and not applicable to non-master devices. This register indicates how long the master would like to retain PCI Bus ownership whenever it initiates a transaction. The value hardwired into this register indicates how long a burst period the device needs (in increments of 250 ns). A value of zero indicates the device has no stringent requirements in this area. This information is useful in programming the algorithm to be used in the PCI Bus arbiter (if it is programmable).

Max_Lat Register

This register is assigned by Conexant. The value is 00.

This register is optional for a bus master and not applicable to non-master devices. The specification states that this read-only register specifies "how often" the device needs access to the PCI Bus (in increments of 250 ns). A value of zero indicates the device has no stringent requirements for the data. This register could be used to determine the priority-level the bus arbiter assigns to the master.

PMC [8:6] and PME DRV Type

These fields are assigned by Conexant.

PMC [8:6]: This 3- bit field reports the 3.3Vaux auxiliary current requirements for the PCI function. If the Data Register has been implemented by this function then 1) reads of this field must return a value of "000b" 2) Data Register takes precedence over this field for 3.3Vaux current requirements. If PME# generation from D3cold is not supported by the function (PMC(15)=0), then this field must return a value of "000b" when read. The value is 000b.

PME DRV Type: This bit sets the driving capability of the PME pin (0 = active high TTL, 1 = active low Open Drain). The value is 1.

Class Code Register (Class Code, Sub-class Code, Prog. I/F)

This register is always mandatory and is assigned by Conexant. The value is 07 for Class Code, 80 for Sub-class code, and 00 for Prog. I/F.

This register is a 24-bit read-only register divided into three sub-registers: base class, sub-class, and Prog. I/F (programming interface). The register identifies the basic function of the device via the base class (i.e. for modems: Simple Communications Controller), a more specific device sub-class (i.e. for modems: Other Communications Device), and in some cases a register-specific programming interface (not used for modems).

CardBus CIS Pointer (CardBus CIS pointer High, CardBus CIS pointer Low)

This register is optional and is assigned by Conexant. The value is 00000000.

This optional register is implemented by devices that share silicon between CardBus and PCI. This field points to the card information structure, or CIS, for the CardBus card. This register is read-only and contains the offset of the CIS.

Data Scale PMCSR[14:13] (D0C, D1C, D2C, D3C, D0D, D1D, D2D, D3D)

This value is supplied by the OEM since Conexant implements the Data Register. Until these values are assigned, Conexant uses a default value 0000.

This field is required for any function that implements the Data Register. The data scale is a 2- bit read-only field which indicates the scaling factor to be used when interpreting the value of the Data Register. The value and meaning of this field will vary depending on which data value has been selected by the Data_Select field (PMCSR[12:09]). There are 4 data scales to select 1) 0 = unknown 2) 1 = 0.1x, 3) 2 = 0.01x, 4) 3 = 0.001x where x is defined by the Data Select Field.

Data Register (D3, D2, D1, D0 power consumed and D3, D2, D1, D0 power dissipated)

This value is supplied by the OEM since Conexant implements the Data Register. Until these values are assigned, Conexant uses a default value of 0000000000000000.

The Data Register is an optional, 8-bit read-only register that provides a mechanism for the function to report state dependent operating data such as power consumed or heat dissipation. Typically the data returned through the Data register is a static copy (look up table, for example) of the function's worst case "DC characteristics" data sheet. This data, when made available to system software could then be used to intelligently make decisions about power budgeting, cooling requirements, etc. The data returned by the data register is selected by the Data Select field (PMCSR[12:09]).

Load CISRAM Count (CIS _SIZE)

This register is optional and is assigned by Conexant. The value is 00.

This register contains an 8-bit value indicating the number of double words to be loaded into the CISRAM for CardBus support.

PMC[15:9, 5] (D3_Cold, D3_Hot, D2, D1, D0, D2_Support, D1_Support, DSI)

PMC[15:11]: PME_Support (D3_Cold, D3_Hot, D2, D1, D0)- This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. D2 and D1 must be 0 since the modem does not support these states. The rest of the values are supplied by the OEM and the values depend upon the systems in which the modem will be installed. Conexant uses a default value of 49. This is for a system which does not support D3cold but supports D3hot.

When D3_Cold is a 1, PMC[15] is set to a 1 if VauxDET is high at device power on reset (POR) or is reset to a 0 if VauxDET is low at POR. When D3_Cold is a 0, PMC[15] is always 0, regardless of the VauxDET level.

PMC[10] (D2_Support): If this bit is a 1 then function supports the D2 Power Management State. Currently the modems do not support this state and therefore this field must be 0.

PMC[9] (D1_Support): If this bit is a 1 then function supports the D1 Power Management State. Currently the modems do not support this state and therefore this field must be 0.

DSI: The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. This bit should always be set to "1".

NOTE: For more information, refer to PCI Bus Power Management Interface Specification.

NOTES

(Inside Back Cover)

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